UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Applied Physics**

Arrêté ministérial : 7 août 2006

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préparée au sein **CEA-LETI**
et de **Ecole Doctorale de Physique, Grenoble**

Scaling Beyond Moore: Single Electron Transistor and Single Atom Transistor Integration on CMOS

Thèse soutenue publiquement le **27th September 2012**,
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Abstract

Continuous scaling of MOSFET dimensions has led us to the era of nanoelectronics. Multigate FET (MuGFET) architecture with 'nanowire channel' is being considered as one feasible enabler of MOSFET scaling to end-of-roadmap. Alongside classical CMOS or Moore's law scaling, many novel device proposals exploiting nanoscale phenomena have been made either. Single Electron Transistor (SET), with its unique 'Coulomb Blockade' phenomena, and Single Atom Transistor (SAT), as an ultimately scaled transistor, are prime nanoelectronic devices for novel applications like multivalued logic, quantum computing etc. Though SET was initially proposed as a substitute for CMOS ('Beyond CMOS device'), it is now widely considered as a compliment to CMOS technology to enable novel functional circuits. However, the low operation temperature and non-CMOS fabrication process have been major limitations for SET integration with FET.

This thesis makes an effort at combining scaled CMOS, SET and SAT through a single integration scheme enabling trigate nanowire-FET, SET or SAT. In this work, for the first time, fabrication of room temperature operating SET on state-of-the-art SOI CMOS technology (featuring high-k/metal gate) is demonstrated. Room temperature operation of SET requires an island (or channel) with dimensions of 5 nm or less. This is achieved through reduction of trigated nanowire channel to around 5 nm in width. Further study of carrier transport mechanisms in the device is carried out through cryogenic conductance measurements. Three dimensional NEGF simulations are also employed to optimize SET design. As a step further, cointegration of FDSOI MOSFET and SET on the same die is carried out. Room temperature hybrid SET-FET circuits enabling amplification of SET current to milliampere range (proposed as 'SETMOS device'

in literature), negative differential resistance (NDR) and multivalued logic are shown.

Alongside, on the same technology, a Single Atom Transistor working at cryogenic temperature is also demonstrated. This is achieved through scaling of MOSFET channel length to around 10 nm that enables having a single dopant atom in channel (diffused from source or drain). At low temperature, electron transport through the energy state of this single dopant is studied. These devices also work as scaled MOSFETs at room temperature. Therefore, a novel analysis method is developed correlating 300 K characteristics with cryogenic measurements to understand the impact of single dopant on scaled MOSFET at room temperature.

Résumé en français

La réduction (“scaling”) continue des dimensions des transistors MOSFET nous a conduits à l’ère de la nanoélectronique. Le transistor à effet de champ multi-grilles (MultiGate FET, MuGFET) avec l’architecture “nanofil canal” est considéré comme un candidat possible pour le scaling des MOSFET jusqu’à la fin de la roadmap. Parallèlement au scaling des CMOS classiques ou scaling suivant la loi de Moore, de nombreuses propositions de nouveaux dispositifs, exploitant des phénomènes nanométriques, ont été faites. Ainsi, le transistor monoélectronique (SET), utilisant le phénomène de “blocage de Coulomb”, et le transistor à atome unique (SAT), en tant que transistors de dimensions ultimes, sont les premiers dispositifs nanoélectroniques visant de nouvelles applications comme la logique à valeurs multiples ou l’informatique quantique. Bien que le SET a été initialement proposé comme un substitut au CMOS (“Au-delà du dispositif CMOS”), il est maintenant largement considéré comme un complément à la technologie CMOS permettant de nouveaux circuits fonctionnels. Toutefois, la faible température de fonctionnement et la fabrication incompatible avec le procédé CMOS ont été des contraintes majeures pour l’intégration SET avec la technologie FET industrielle. Cette thèse répond à ce problème en combinant les technologies CMOS de dimensions réduites, SET et SAT par le biais d’un schéma d’intégration unique afin de fabriquer des transistors “Trigate” nanofil. Dans ce travail, pour la première fois, un SET fonctionnant à température ambiante et fabriqués à partir de technologies CMOS SOI à l’état de l’art (incluant high-k/grille métallique) est démontré. Le fonctionnement à température ambiante du SET nécessite une le (ou canal) de dimensions inférieures à 5 nm. Ce résultat est obtenu grce à la réduction du canal nanofil ”trigate” à environ 5 nm de largeur. Une étude plus approfondie des mécanismes de transport mis en jeu dans le dispositif est réalisée au moyen de mesures cryogéniques de conductance. Des simulations NEGF tridimensionnelles sont également utilisées pour optimiser la conception du SET. De plus, la cointégration sur la même puce de MOSFET FDSOI et SET est réalisée. Des circuits hybrides SET-FET fonctionnant à température ambiante et permettant l’amplification du courant SET

jusque dans la gamme des milliampères (appelé “dispositif SETMOS” dans la littérature) sont démontrés de même que de la résistance différentielle négative (NDR) et de la logique à valeurs multiples.

Parallèlement, sur la même technologie, un transistor à atome unique fonctionnant à température cryogénique est également démontré. Ceci est obtenu par la réduction de la longueur de canal MOSFET à environ 10 nm, si bien qu'il ne comporte plus qu'un seul atome de dopant dans le canal (diffusée à partir de la source ou de drain). A basse température, le transport d'électrons à travers l'état d'énergie de ce dopant unique est étudié. Ces dispositifs fonctionnent également comme MOSFET à température ambiante. Par conséquent, une nouvelle méthode d'analyse est développée en corrélation avec des caractéristiques à 300K et des mesures cryogéniques pour comprendre l'impact du dopant unique sur les caracteristiques du MOSFET à température ambiante.

To My Parents

Acknowledgements

First of all I heartily thank my advisors Dr. Maud Vinet, Dr. Xavier Jehl, Dr. Romain Wacquez and Dr. Marc Sanquer who gave me an opportunity to carry out my thesis work under their guidance. During the three years of my thesis work, their advice and support was both ever-motivating and illuminating in many difficulties that arose during device fabrication and analysis. Each one of them has played a special role in educating me into a good researcher.

Fabrication of ultrascaled nanowires in CMOS process is a very challenging task. This would not have been possible without the team effort and contribution of various process engineers at LETI clean room, who supported me throughout with great enthusiasm. I thank all of them for helping me successfully complete my thesis work. I would like to extend special thanks to Mr. Bernard Previtali and Mr. Christian Vizioz, who happily involved in the fabrication process, despite the great many difficulties involved, kept pushing the process tools beyond limit to achieve the process targets.

I thank Dr. Sylvain Barraud who in a way 'adopted' me after my advisors at LETI had to leave to US on assignment. His support and guidance has been substantial in my making as a researcher. It had been my aspiration since the beginning of my experimental work to support it through simulations. This wish came to life with the support from Dr. Francois Triozon, who was kind to try out some of my naive ideas in the simulator he has developed. Thank you very much. Discussions with you helped me learn a great deal about nano device simulations. I also thank Dr. Olivier Weber, Dr. Francois Andrieu, Dr. Cyril LeRoyer, Dr. Perrine Batude, Dr. Thierry Poiroux who gave professional advise on MOSFET device technology. I am grateful to my lab heads Dr. Olivier Faynot and Dr. Barbara De Salvo for

their constant encouragement and support. Thanks to Prof. Alexei Orlov for the nice discussions on the SET physics.

I heartily thank my jury, Prof. Bournel, Prof. Souifi, Prof. Delerue, Prof. Fanciulli, Dr. Magnea for their kind acceptance to be in my defense committee.

Manan, Quentin, Cuiqin, Louis, Milene, Guilleaume, Carlos who shared the roller-coster ride of thesis work in the same 'bureau de thesards', many thanks to you. My time would not have been fun without you. Manan for specifically sharing all those 'analyst' evenings pondering over world problems, formulating our own solutions. Thousands of 'potential startups' capable of revolutionizing the world have been made in due process. Nitin, Sandeep and Prem for being there in all the fun days of Grenoble life. Benoit Roche, Benoit Voisin and Byron, thanks a lot for your constant help fixing things in the lab. Thanks to all friends near and far for all the joyous moments.

Last but not least, I heartily thank the constant support of my parents, my sisters and my girlfriend who have kept up my spirits throughout. Without their care and encouragement I would not have been able to tread a path so long.

This work would not have been possible without the scholarship support from CEA, my thanks to selecting me for the CFR scholarship.

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1

Introduction

1.1 Context

The invention of integrated circuits in 1959 was a milestone event that led to birth and development of modern semiconductor industry. Integrated circuits enabled invention of new functional devices and gadgets that have improved quality of life in general. Multifunctional devices built from complex ICs fabricated on CMOS technology are now ubiquitous. This has only been possible due to the ability to add more components in ICs making them more dense and complex. The driving force behind this ever increasing complexity and density of ICs is the ever shrinking size of their basic component: the MOSFET. Back in 1965 Gordon Moore envisioned the economics of increasing complexity and proposed [Moor 65] the famous Moore's law: "Increasing the integration density by factor of two a year would minimize the cost per transistor". Owing to this commercial incentive the semiconductor industry has since been trying to follow this law. On the technological side this meant the necessity to reduce the transistor dimensions keeping its basic structure intact. To this end, Dennard [Denn 74] proposed some scaling rules that would lead to a gain in performance of the transistor on size reduction. On these guidelines the scaling of the MOSFET (specifically the gate length) continued without hindrance from 100 μm size to 100 nm. On reaching 100 nm (or the deep sub-micron channel length), maintaining the electrostatic integrity of the transistor became a major issue leading to serious challenges to scaling. Some of the major problems to MOSFET scaling in sub-100 nm channel length regime are:

1. Short channel effect (SCE).

2. Drain induced barrier lowering (DIBL).

3. Increased off state current.

4. Increased gate leakage.

5. Poly gate depletion effects.

6. Source/Drain access resistance reduction.

7. High field mobility degradation.

8. Variability.

In order to overcome these challenges significant innovations were made at every new technological node. We saw introduction of new materials and architectures for the MOSFET in the last decade. To mitigate polysilicon depletion effect, polysilicon gate was replaced with metal gate. Alongside, as the gate leakage also became a serious issue due to tunneling current through thin SiO_2 layer, the gate oxide was replaced with high-k dielectric material (HfSiON, HfO_2 etc.)[Mist 07]. Stressor layers were introduced to boost mobility of carriers to counter high field mobility degradation. As the gate length shrank even further, at around 30 nm, short channel effects became very serious requiring paradigm shifts in the MOSFET architecture to continue scaling. Effective gate control on the channel had to be increased considerably to reduce detrimental short channel effects below 30 nm. It has been demonstrated that this could be achieved reliably through multigate FET architecture (as in finFET) or through fabrication of planar FET on ultrathin SOI substrate. Now there is a general consensus that sub-22 nm nodes will require 'fully depleted channel' MOSFETs. Various industries have chosen to employ one of these architectures at sub-32 nm nodes. Recently, for 22 nm node, Intel announced introduction of 'trigate MOSFET' on bulk substrate, thereby going from planar to quasi-planar channel architecture. Whereas ST Microelectronics plans to roll out its 28 nm node devices on FDSOI architecture.

Figure 1.1 shows the evolution of MOSFET technology over time with recent projections from ITRS for the future. Significant changes in material and architecture of MOSFET were observed in sub-100 nm nodes indicating a significant departure from classical scaling. MOSFETs at the end of ITRS roadmap are projected to have gate

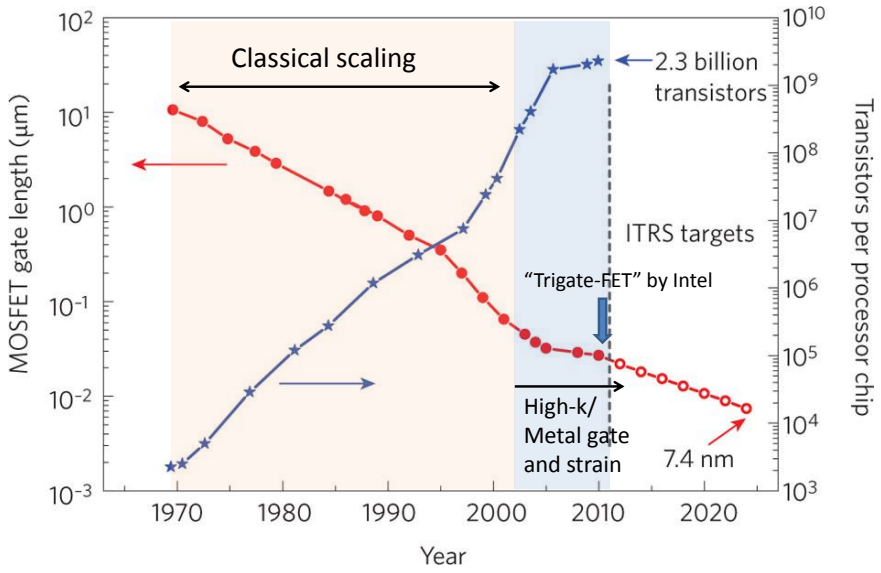


Figure 1.1: Time evolution of MOSFET gate length in microprocessors (adapted from [Schw 10]). ITRS roadmap projections show the gate length to scale down to around 8 nm at the end-of-roadmap.

length around 8 nm. All the approaches employed at 22-28 nm nodes are expected to enable scaling of MOSFET till the end-of-roadmap.

1.1.1 Going *Beyond Moore*

As discussed before, considerable efforts and technological innovations have ensured scaling of MOSFET to end-of-roadmap. The projections of ITRS (Fig.1.1) indicate that at the end-of-roadmap the MOSFET gate length would shrink to about 8 nm or less. Let us consider multigate architecture, specifically trigate FET, to the end-of-roadmap. Scaling rules for trigate devices till the end of roadmap have been studied and analyzed in many simulation works [Yu 08]. It has been predicted that for maintaining excellent electrostatic integrity width (W) of the channel should be at least $L_G/3$. This means that the channel width for trigate devices at the end-of-roadmap would be less than 5 nm. Thus the channel would naturally evolve into a 'nanowire' channel. Therefore end-of-roadmap trigate MOSFETs will actually be trigate nanowire MOSFETs. Reduced channel width in nanowires implies lesser cross sectional area or

channel volume and hence lesser number of carriers that contribute to conductance. Reduced number of carriers in turn means that the quantized nature of charge starts affecting the device characteristics. Also the importance of disorder (potential fluctuations) increases drastically as one goes to 1D channel, especially with respect to source (S)/ drain (D)-channel junction. Extreme case of this is a single charge determining the transport through the device! Hence it can become a serious challenge to the basic functionality of the MOSFET itself when end-of-roadmap dimensions are reached. However, by innovative engineering of the device, this challenge can be turned into an opportunity. This can be achieved through a device whose functionality depends on discreteness of the charge. Such a device that controls the flow of single electrons, known as the Single Electron Transistor, was proposed in 1986 [Aver 86] and has since been studied extensively by physicists. As the name suggests, it is a transistor whose transfer characteristics are due to single electron addition to the channel. Schematic of the SET structure, as proposed, is shown in figure 1.2a. As seen from the figure the SET was proposed to be different from the MOSFET. The channel of SET is a nanoscale "island" separated from the source and drain by tunnel barriers. Gate controls tunneling of electrons across these tunnel barriers leading to conduction. Figure 1.2b shows the circuit schematic of the SET. Tunnel barrier capacitance and resistance are denoted C_S (C_D) and R_S (R_D) for source (drain). The gate capacitance is denoted C_G. Details of

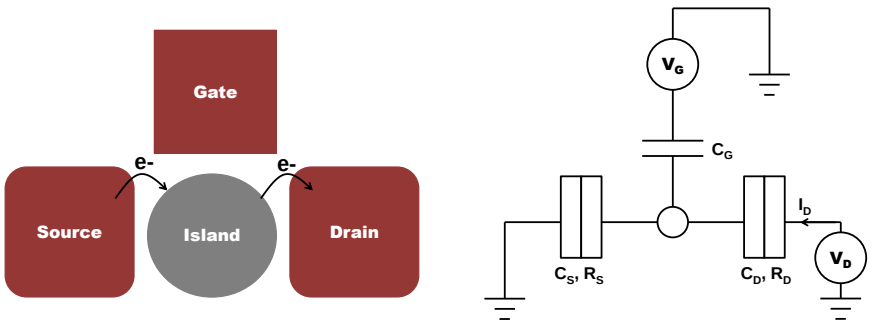


Figure 1.2: (a)Schematic of SET.(b)Schematic of equivalent circuit for SET

carrier transport and electrical characteristics of SET will be discussed in next chapter.

1.2 Outline

In this work we demonstrate that a SET, a seemingly different device, can be engineered from an extremely scaled nanowire (NW)-MOSFET. Thereby we show the possibility of SET-FET cointegration on state-of-the-art CMOS technology, providing a pathway for going *beyond Moore*, when MOSFET scaling reaches end-of-the roadmap. Unlike the popular viewpoint of SET as a non-CMOS or beyond CMOS device, we propose to integrate it well within the CMOS technology (and within the roadmap!) fostering a synergic technological development for both, end-of-roadmap MOSFET and SET to add novel functionalities hitherto absent in classical Moore scaling.

In chapter 2 the basic theory of transport physics in SET and its fabrication is outlined. The main parameters of SET critical for practical applications (charging energy, island size etc.) are identified. Based on these factors, an overview of various efforts at SET fabrication is given, with specific focus on Si based room temperature operating SETs.

In chapter 3 our approach to SET integration on CMOS is described. We demonstrate a single integration scheme to realize nanowire (NW)-MOSFETs and room temperature operating SET. The characteristics NW-MOSFETs fabricated within this integration scheme are then presented. Devices with room temperature SET characteristics are shown and the origin of the characteristics is discussed in detail. Low temperature measurements are also presented and discussed in the light of various transport mechanisms. Finally, various solutions for realizing well-controlled, room temperature operating SET on CMOS are proposed.

Having shown room temperature operating SET on CMOS integration scheme in chapter 3, going a step further, the cointegration of SET and FET is demonstrated in chapter 4. Various hybrid SET-FET circuits, proposed earlier by circuit designers, are demonstrated at room temperature and various parameters that influence the circuit performance are discussed in detail.

In chapter 5 another aspect of scaling, the gate length scaling is considered. As gate length of MOSFET is scaled, source-drain are brought very close together. So the device structures resembles two contacts connecting a small section of silicon. If a single dopant atom is placed in this section of silicon, it would be equivalent to contacting the dopant with two electrodes and a gate to control the conductance. Therefore by

pushing gate length scaling to the limits (end-of-roadmap dimensions), single atom transistor working at low temperature is demonstrated. The role this single dopant plays on the room temperature characteristics of these ultrascaled gate length FETs is also discussed in detail.

Finally, in chapter 6 we give conclusions on our work and provide perspectives on possible paths in future for robust SET integration.

2

SET Basics: Physics and Technology

In this chapter, in the first section the basic theory of transport in SET is built from the concept of Coulomb Blockade. Conductance through SET is described on the lines of *orthodox theory* in the metallic limit. From the physics of the device main parameters of SET critical for practical applications are identified, specifically the operating temperature requirement. As will be seen, the operating temperature of SET is a major challenge for practical applications. Therefore, major efforts that have been done to improve the operating temperature of SET are mentioned and briefly discussed.

2.1 SET Device Basics: Requirements for 300 K Operation

The basics of single electronics is based on the concept of Coulomb blockade (CB). Consider a small neutral metallic conductor, for simplicity, a sphere in vacuum. Adding one electron to it raises its charge by $-e$. Now an electric field builds up due to charging of the sphere. This field repulses the electrons to be added subsequently ($\vec{F} = -e\vec{E}$). So certain work has to be done in order to add next electron. If 'C' be the total capacitance of the sphere then the work (W) required to add a new electron (after adding the first one) is:

$$W = \int \vec{F} = \frac{1}{2}CV^2 = \frac{1}{2}C\left(\frac{-e}{C}\right)^2 = \frac{e^2}{2C} \tag{2.1}$$

Since 'C' decreases with the size of the sphere, this energy can be considerable for nanometer scale spheres. For instance a spherical island of diameter d = 100 nm (embedded in SiO_2), has a charging energy: $\frac{e^2}{2\pi\epsilon d} = 7\ meV$. Thus at this scale the effect of single electron addition become prominent.

Now, extending this, consider a nanometer scale metallic sphere (in practice a metallic grain and conventionally called island) weakly connected by two leads or contacts (called source and drain) which can act as reservoirs of electrons to charge the island through a voltage 'V' across them. Since it is required to keep the electrons confined to the island, yet allow electron transfer across, we have to have tunnel barriers between the island and the leads. Add another electrode (gate) on the island to control its potential by applying voltage to it. We can now make electrons tunnel into the island, charge it. To add more electrons we need to overcome the Coulomb repulsion, so use the third electrode to change potential of the island thereby letting more electrons. Slight bias across the source-drain electrodes gives preferential direction for electrons to flow. This flow can be controlled by third electrode. So what we effectively create is a device that lets the electrons flow one by one across the island and the tunnel barriers. This is similar to the conventional MOSFET albeit with the ability to charge the channel ('island') with just one electron. Therefore the device is named SET- Single Electron Transistor.

2.1.1 SET Transport Physics

As seen before, the prominence of single electron charging effect is measured by the electrostatic work (W) required. This is conventionally called as the 'charging energy', denoted E_c. It is evident that this energy is of considerable level (of practical voltage levels) when the island is of nanometer size. Also, in such small conductors if the de Broglie wavelength of the electron becomes comparable to the size of the conductor then quantum mechanical effects become important. They can be characterized by another energy E_k, the quantum kinetic energy of added electron. Therefore, the total energy, called addition energy E_a, can be estimated as:

$$E_a = E_c + E_k \tag{2.2}$$

This represents the total electrostatic work to be done to add an additional electron to the island. For single electron effects to be observable and controllable the thermal

energy should be less than the charging energy. So as a practical estimate the addition energy should satisfy at least:

$$E_a \geq 10kT \tag{2.3}$$

where T is the absolute temperature. It will be seen that charging energy becomes the prime criteria for qualifying SET for practical device applications. Most of the effects in single electronics are explained quantitatively (for metallic based SETs) and qualitatively (for small semiconductor based SETs) by "orthodox" theory developed by Kulik and Shekhter[Kuli 75] and later generalized by others. The major assumptions of the theory are:

1. Electron energy quantization inside the conductors is ignored. This is valid only when the energy levels E_k of electrons are smaller than E_c. Hence valid for metallic islands and inadequate for very small semiconductor islands. For example in a $S = 1\ \mu m^2$ GaAs 2DEG island, quantized energy level separation ($\Delta_1 = \frac{2\pi\hbar^2}{4mS}$ where m is effective mass) is 0.1 meV.

2. Time (τ) of electron tunneling through the barriers is smaller than all other process times involved. This is true for the SETs under study, where $\tau = 10^{-15}$ s [Likh 99].

3. Higher order quantum processes such as 'cotunneling', which involves multiple tunnel events simultaneously, are ignored. As a thumb rule for island to be capable of confining electrons the following relation should hold:

$$R_T = \frac{\hbar}{e^2} \sim 26\ k\Omega \tag{2.4}$$

   where R_T is the resistance of the tunnel barriers. Therefore, one can notice that SET is inherently a high impedance device contrary to MOSFET which is a low impedance device. We will see later that this becomes one major challenge for SET applications in digital logic.

A handwaving argument for the above condition can be given on basis of Heisenberg energy uncertainty relation:

$$\Delta E \Delta t \geq \frac{\hbar}{2} \tag{2.5}$$

Combining this with the tunnel event of one charge where charging energy can be the energy uncertainty and 'R_TC' (charging time of the tunnel junction) as the time

uncertainty, we obtain equation 2.4. With these assumptions, the theory explains the transport characteristics of single charge tunneling devices. Tunneling is a random event with a certain rate Γ, which depends on the reduction of free energy (ΔW) of the system as a result of tunneling. In general:

$$\Gamma(\Delta W) = \frac{I\Delta W}{e^2\left(1 - exp\left(\frac{-\Delta W}{k_B T}\right)\right)} \tag{2.6}$$

where I(V) is the dc I-V curve of the tunnel barrier in absence of single-electron charging. ΔW depends on the system under consideration. Our system is the single electron transistor. Figure 2.1 shows the SET circuit. As seen in the figure, the island has two tunnel barriers on either side. The potential of the island is further controlled by a capacitively coupled gate electrode. Under the assumptions defined above, we can now study the transport across SET in the framework of orthodox theory. The net free energy change for tunneling event across the two tunnel barriers determines transfer characteristics of the device. Only those tunneling events that lead to lowering of free energy are allowed. Hence we will now evaluate the free energy change for a tunneling event to get the conditions for stable operation.

Using the same conventions as for the classical MOSFET, the two terminals of SET can be called source and drain. The tunnel capacitance and resistance for source (drain) tunnel junction are C_S (C_D) and R_S (R_D) respectively. Let us consider an external applied voltage 'V_{DS}' across the two tunnel barriers. So $V_{DS} = V_S + V_D$,

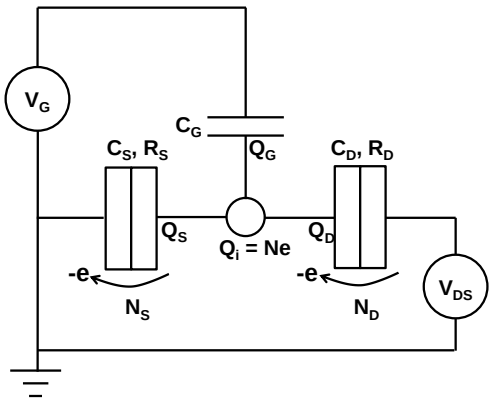


Figure 2.1: Circuit diagram of SET showing charges on all capacitors and tunneling events considered.

where V_S and V_D are internal voltage drops across the source and drain tunnel junctions respectively. The charges on the source and drain capacitors will be Q_S ($=C_S V_S$) and Q_D ($=C_D V_D$). Let C_G be the gate capacitance with a voltage 'V_G' applied to it. The total capacitance of the island is: $C_\Sigma = C_S + C_D + C_G$. The net charge on the island is therefore:

$$Q_{net} = (Ne - C_S V_S - C_D V_D - C_G V_G) \tag{2.7}$$

where, N is the electron number (or occupation number) on the island. Hence the net electrostatic energy of the island is:

$$W_N = \frac{Q^2{}_{net}}{2C_\Sigma} = \frac{(Ne - C_S V_S - C_D V_D - C_G V_G)^2}{2C_\Sigma} \tag{2.8}$$

Since the source is kept at ground, the potential of the island will given by:

$$W_N = (C_S V_S + C_D V_D + C_G V_G - Ne)C_\Sigma \tag{2.9}$$

Now as the electron number of the island changes due to tunneling across either of the junction, the net electrostatic energy of the island changes. This change is the change in free energy of the island. We can define a 'chemical potential' for the island that reflects the change in its occupation number[1]. It is given by:

$$\mu(N) = W(N) - W(N-1) = \frac{e^2}{C_\Sigma}(N + \frac{1}{2} - \frac{(C_S V_S + C_D V_D + C_G V_G - Ne)}{e} \tag{2.10}$$

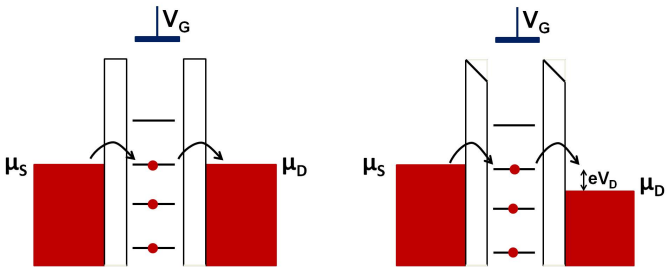
Based on this equation we can have energy levels associated with single electron charging of the island as shown in figure 2.2a. The levels are equally spaced with a spacing given by the charging energy, E_c which is given by:

$$E_c = \frac{e^2}{C_\Sigma} \tag{2.11}$$

Therefore, for a SET to have CB at room temperature the charging energy should be higher than 26 meV (thermal energy). This implies that the total capacitance of the SET should be few aF.

We would like to stress a point here. This energy level diagram is solely derived from chemical potential that results from capacitive charging of the island. Therefore it is not related to 'quantum confined levels' resulting from quantum mechanical nature of

[1]This chemical potential is different from the material chemical potential of the island that is intrinsic to the island.



(a) Charging level aligned to source chemical potential by V_G.

(b) Charging level aligned to source chemical potential by V_D.

Figure 2.2: Charging energy level representation for the island.

electron in the island. Single electron charging and Coulomb blockade are not quantum effects but result of classical electrostatic charging of the island! So a SET is not be confused as a 'quantum device' unlike a resonant tunneling diode (RTD) the works on the energy levels formed by 2D 'quantum confined' electron system.

2.1.2 $I_D - V_G$ Characteristics of SET

Consider that the applied voltage across the source-drain tunnel barriers (V_{DS}) is very small rather almost zero. The gate voltage can then viewed as a handle to shift the charging energy levels of the island (figure 2.2a) with respect to the fermi level in the source and drain. So when a level aligns with the fermi level of source an electron can tunnel into the island and subsequently tunnel out to drain[1]. Thus the SET will be in conducting state or 'ON' state. When the gate voltage is changed the levels are no longer aligned and there is no conduction. This gives the 'OFF' state for the SET. So we have the $I_D - V_G$ characteristics of the SET as shown in figure 2.3. It is periodically peaked curve with each peak changing the occupation number of the island by one electron. Therefore the peak separation has a period equal to:

$$\Delta V_G = \frac{e}{C_G} \tag{2.12}$$

Thus the spacing of peaks measured in experiments gives us the gate capacitance of the SET. We have seen that the tunneling rate across the barriers depends on the free

[1]These tunneling events are only spatially correlated and have no temporal correlation. In and out tunneling events are completely random.

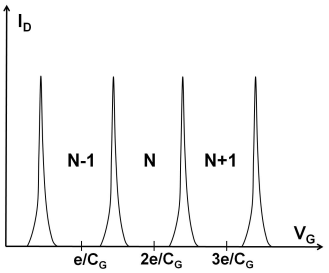


Figure 2.3: Typical $I_D - V_G$ characteristics of a SET at very small drain bias, $V_{DS} \sim 0$ and finite temperature (which gives the line width for the peaks).

energy change associated with a tunnel event (Eqn. 2.6). This expression of tunnel rate also includes the resistance (or the conductance) of the barrier. Substituting the free energy change (Eqn. 2.10) in it and from the master equation [Been 91] one can derive expression for conductance in linear regime, G ($=\frac{I}{V}$, with $V \to 0$) as:

$$G = \frac{1}{2}\frac{G_S G_D}{G_S + G_D}\frac{\frac{e\alpha V_G}{k_B T}}{sinh\left(\frac{e\alpha V_G}{k_B T}\right)} \tag{2.13}$$

where α is the 'lever arm factor' of the gate given by:

$$\alpha = \frac{C_G}{C_\Sigma} \tag{2.14}$$

The evolution of conductance of the Coulomb blockade peak with temperature, given by equation 2.13 is plotted in figure 2.4. It can be seen that the peak amplitude remains the same for various temperature as long as $E_c > k_B T$. Only the width of CB peak increases as fermi distribution of electrons at higher temperature gives access to more states for tunneling.

2.1.3 $I_D - V_D$ Characteristics of SET

We will now look at the conditions that qualitatively explain the $I_D - V_D$ characteristics of a SET. Consider a gate voltage for which the charging level of the island is not aligned with the chemical potential of the source/drain. In this case there is no current as shown in figure. Now when a drain voltage is applied, the chemical potential of the drain is lowered and the voltage drop across the barriers also lowers the charging level in the island. As soon as the charging level aligns with the chemical potential of the source, electrons can tunnel into the island and then out to drain (figure 2.2b). Thus the SET

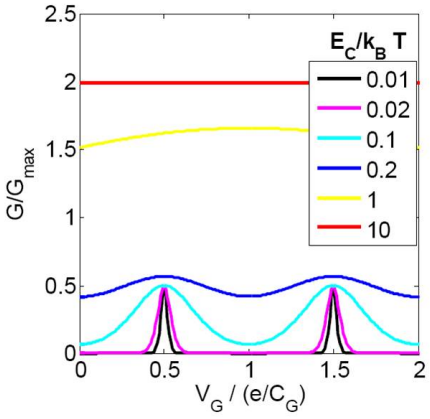


Figure 2.4: $G - V_G$ curves of a SET at very small bias $V_{DS} \sim 0$ for various temperatures taken as the ratio: $\frac{E_c}{k_B T}$. Here $G_{max} = \frac{G_S G_D}{G_S + G_D}$.

starts conducting. So we also see that there is threshold voltage above which the SET conducts. It can be seen that this voltage is equal to: $\frac{e}{C_\Sigma}$. Therefore we have $I_D - V_D$ characteristics of the SET as shown in figure 2.5. Here we see a threshold voltage beyond which the SET starts conducting. The region below this threshold is known as the 'Coulomb blockade region', arising due the Coulomb blockade effect. Having seen

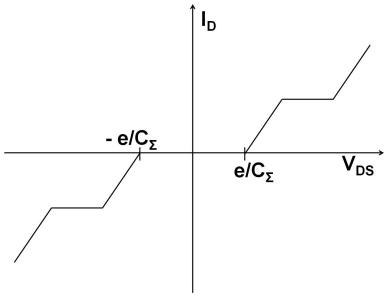


Figure 2.5: Typical $I_D - V_D$ characteristics of a SET.

both the $I_D - V_G$ and $I_D - V_D$ characteristics of the SET, we can now see the combined characteristics. When the gate voltage of the SET is changed along with the drain voltage, the drain current as a function of V_G and V_{DS} can be plotted as a 2D color plot generally known as 'stability diagram' or 'Coulomb diamond plot' of the SET. It is shown in figure 2.6. The diamond like regions in the plot represent the bias conditions when there is no current through the device. The slopes of the diamond depend on the source, drain and gate capacitances (slopes are shown on the figure). From the

measured 'Coulomb diamond' slopes of a SET one can thus calculate the source and drain capacitances.

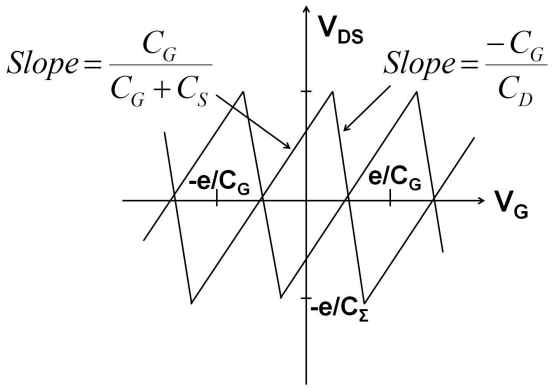


Figure 2.6: Typical Coulomb diamond plot for a SET. The slopes give source, drain capacitances and half the height of diamond from V_G axis gives the charging energy.

From the discussion one can note that a charging energy (E_c) greater than 26 meV and tunnel resistances higher than 26 kΩ as necessary conditions for room temperature operation. However, these are not necessarily sufficient conditions as in the discussion we have only considered tunnel barrier resistance to be independent of temperature and applied voltages. In practice higher values for E_c (typically 100 meV) and tunnel resistance (few hundred kΩ) are required.

2.2 SET Fabrication: What has been done before

In the preceding section we looked at the working of a SET. We will now turn our attention to the fabrication of SET. The theory of single electron transistor developed in the last section was quite general and was independent of material properties. Therefore, one can safely assume that a SET can be made from any conducting material (with suitable tunnel barriers) as long as the basic structure can be fabricated from it. Since room temperature operation requires islands of size less than 10 nm, orthodox theory may no longer be valid if quantized level separation in such islands is considerable. Therefore the theory is sufficient to explain metallic island but not semiconducting island/dot based SETs [Been 91]. Despite these differences, the basic transfer characteristics that are important to realize SET based digital/analog circuits are similar

in both cases. Therefore, on a general note we rather focus on those parts of the device that are critical to realize room temperature operation and large circuits (both pure SET based circuits and hybrid SET-FET circuits). One can broadly identify the following as important requirements for any SET fabrication scheme to this end:

1. Channel or island size: Size of the island is the primary factor that determines the operating temperature of SET. We have seen in the previous section that charging energy consideration demands an island/channel dimension of nearly 5 nm for room temperature operation. Therefore SET fabrication technology should be capable of fabricating a channel of at least 5-10 nm size (diameter for spherical, edge length for rectangular channels).

2. Optimal tunnel barriers: As seen in the last section, the minimum resistance of tunnel barriers should be at least 26 kΩ. But to enable efficient digital/analog circuit operations thermally activated tunneling has to be blocked. So the practical requirements for barrier resistance are much higher (about 5 times quantum resistance). Also, as the current through the SET depends on tunnel resistance, it should not be 'too high' as well. For room temperature operating SETs it is usual and acceptable to have resistances from 100 kΩ to about a couple of MΩ. Besides, an ideal barrier would have a fixed barrier height. However, in real materials, it gets modulated by applied voltage. It is better to have a barrier where this effect is minimum. Oxide tunnel barriers in metallic SETs have this advantage.

3. Gate control: It is necessary to have good gate control of the channel, to realize high peak to valley current ratio (PVCR).

4. Scalable and CMOS compatible fabrication technology: In order to realize high density functional circuits using SETs, it is essential to have a reliable fabrication technology that enables fabrication of large number of SETs. Since due to low current drive of SET, hybrid SET-FET circuits rather than all-SET circuits seem to be more useful. So the SET fabrication technology has to be compatible with CMOS technology. The closer it is to CMOS technology the better it is, the best case being SET fabricated in CMOS technology.

Considering these factors, few schemes of SET fabrication in different materials (and different SET types) are briefly described in the next sections. There are vast number

of research works that have demonstrated SETs through different fabrication methods. However, in the following sections only those works that have demonstrated controlled fabrication, higher operation temperature and CMOS compatibility, to the best of our knowledge, are discussed. 2DEG based SET is an exception to this. It has been mentioned for historical reasons.

2.2.1 Metallic and 2DEG SET

Generally, metallic SETs are made of aluminium (though other metals have been explored). A grain of aluminium acts as island and Al electrodes act as source and drain. The tunnel barriers are formed by aluminium oxide. In fact the first experimental demonstration of SET concept by Fulton and Dolan [Fult 87] was through such a metallic SET. It is made by shadow mask and two angle evaporation process, wherein two layers of aluminium are evaporated successively from two angles through a single suspended mask. The mask has nanometer scale structures. These structures are obtained by e-beam lithography and development of resist. The details of the process are shown in figure 2.7. Figure 2.8 shows SEM image a SET made by a modified version of this approach by Nakamura et al [Naka 96]. The $I_D - V_G$ curves of the device are as shown in the figure 2.9a, and figure 2.9b shows the Coulomb diamonds of the device with a charging energy of 23 meV. The corresponding capacitances are $C_S =$

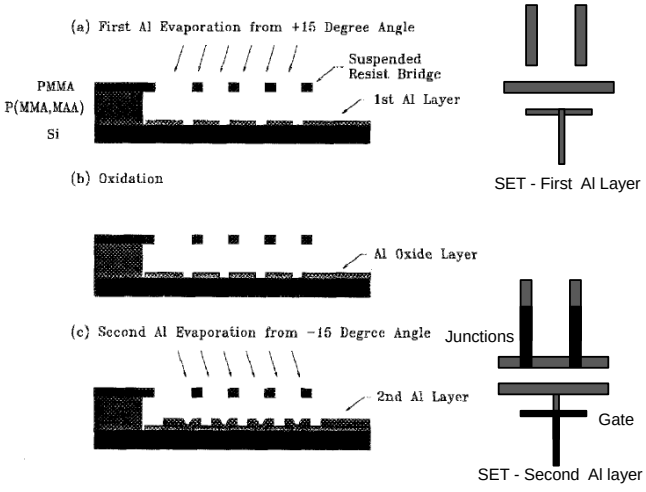


Figure 2.7: Schematic showing Al/AlOx metallic SET fabrication process flow. Adapted from [Ji 94].

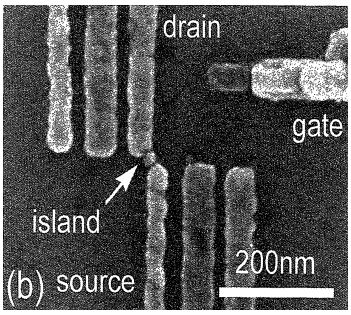


Figure 2.8: SEM image of Al/AlOx SET [Naka 96]

4 aF, $C_D = 2.9$ aF and $C_G = 0.13$ aF. Owing to small total capacitance, the charging energy is high and the device shows clear Coulomb oscillations up to 100 K. However, it is still well below room temperature operation. Some recent works on metallic SETs have demonstrated characteristics indicating possibilities of room temperature operation. One among them is the 'nanodamascene process' developed by researchers at University of Sherbrook[Dubu 08], wherein a Ti/TiO_x based SET has been fabricated and electrical characteristics indicating possibility of room temperature operation have been demonstrated. Though all the materials used in Al based SET are fully CMOS compatible, the fabrication steps can not be included in standard CMOS process flow as it introduces immense complexity in front-end integration schemes. In order to fabricate SET-FET circuits one has to fabricated SET and FET separately in different process steps [Prag 11].

GaAs/AlGaAs interface is known to create a clean 2DEG. By using top gates to selectively deplete parts of the 2DEG, an island can be created with two reservoirs (source and drain) separated by the depletion region. This depletion region plays the role of tunnel barriers. For controlling the potential of the island either additional side gates can be fabricated or the substrate can be polarized to act as back gate. Figure 2.10 shows SEM image of such a SET from ref [Kast 92]. The GaAs/AlGaAs heterostructure is grown using molecular beam epitaxy (MBE). Due to its high quality interface a clean 2DEG with low disorder (mean free path nearly 1μm) is obtained. The $G - V_G$ characteristics of the device are shown in figure 2.11. Here substrate is used as the gate. Clear Coulomb oscillations can be seen in the $G - V_G$ curves. This method is very useful in creating SETs with very well behaved characteristics and has led to

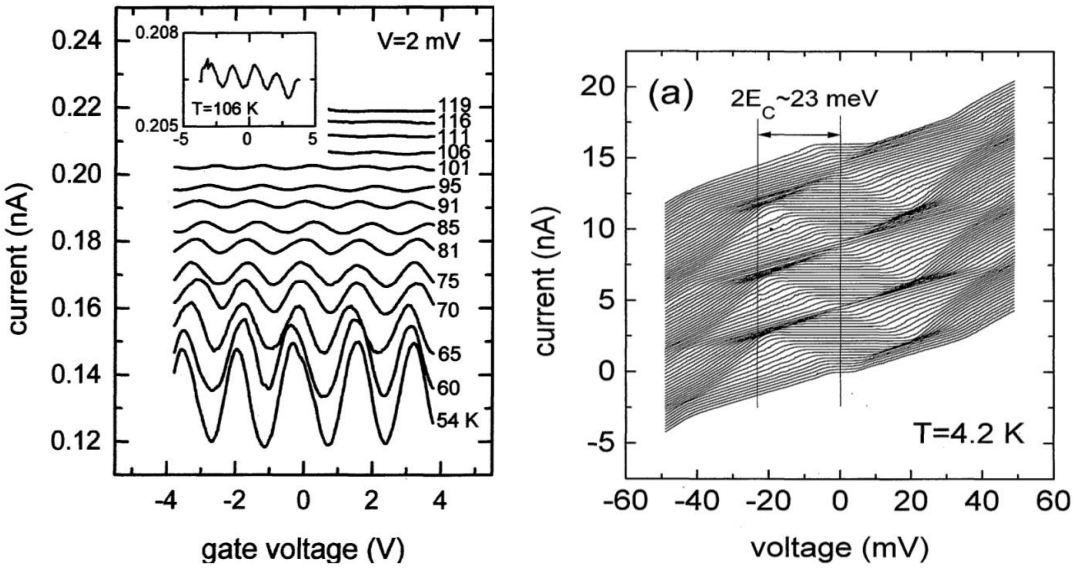


Figure 2.9: (a) $I_D - V_G$ curves for various temperature. Coulomb oscillations are visible below 100 K. (b) Coulomb diamonds for the device. Figure from ref [Naka 96]

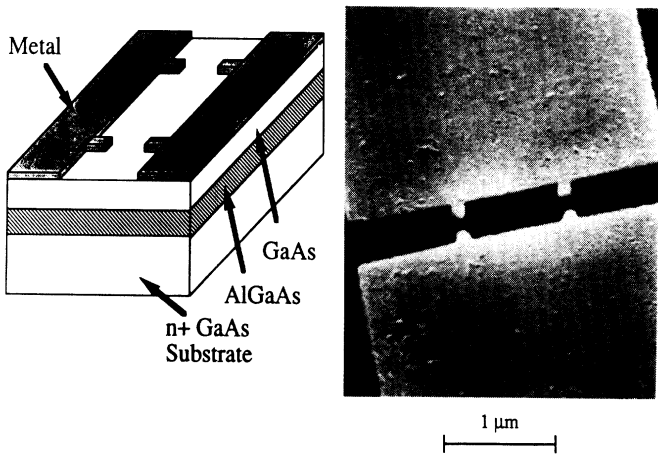


Figure 2.10: SEM image and schematic of material stack of a top gate 2DEG SET [Kast 92].

elucidation of most physics related to single charge tunneling phenomena. However due to the use of exotic materials and multiple gates required this method of fabrication is of limited use to create practical SET based circuits.

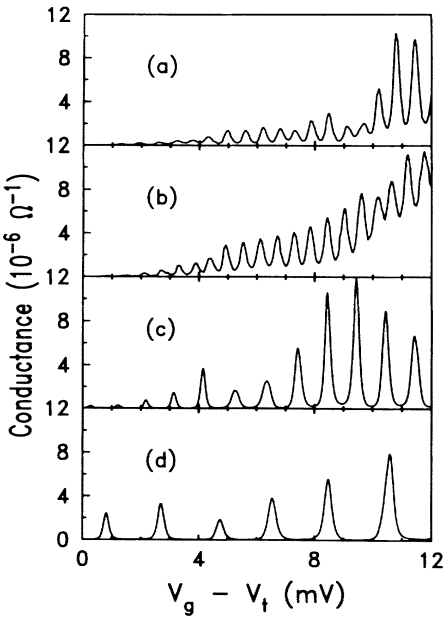
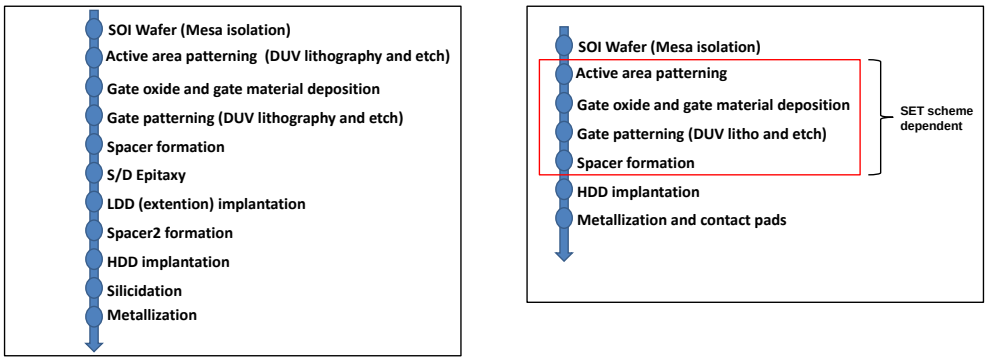


Figure 2.11: $I_D - V_G$ characteristics of the 2DEG SET [Kast 92].

2.2.2 Silicon based SETs

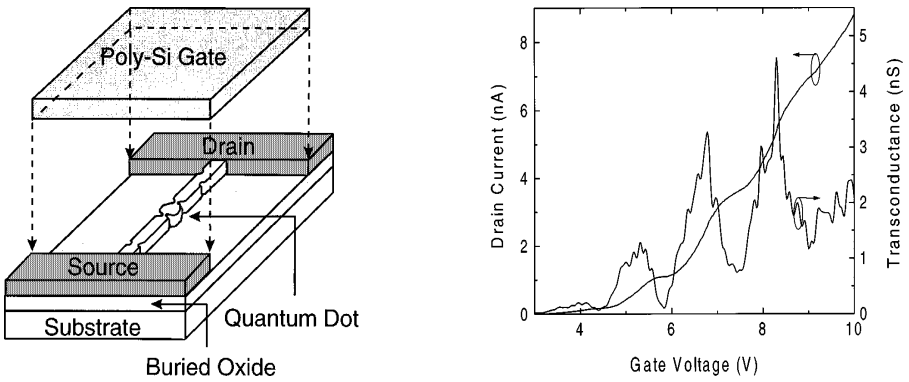
CMOS based IC fabrication has been the biggest technological revolution of 20th century. In order to reap full benefits of the potential applications of SET, it is essential to make its fabrication CMOS compatible so as to enable large volume manufacturing. Therefore naturally the first step was to develop a fabrication process for silicon based SET. Many attempts have been made in this direction. The promising ones are those wherein the conventional SOI-MOSFET fabrication is modified so as to realize a SET. As most of the process steps are the same as in CMOS technology, this general process integration scheme is most likely to lead to large scale SET-FET circuits and applications. Figure 2.12 shows the conventional SOI-MOSFET integration scheme and general modifications done to it to obtain a SOI based SET. Most of the works to be discussed subsequently exploit this approach, each differing in critical steps (boxed in figure 2.12).

One of the first CMOS compatible room temperature SETs [Ishi 96, Guo 97, Taka 95] was made by Chou et al [Zhua 98]. They realized a SET which showed weak coulomb oscillations at 300 K. The schematic of the device is as shown in figure 2.13a. The fabrication was done on SOI substrate. The device is similar to conventional MOSFET



(a) **(b)**

Figure 2.12: (a) Standard SOI-MOSFET process integration scheme. (b) General process steps for SOI based SET. Steps in the box are critical ones that define island and tunnel barriers. Different approaches differ in these steps. Many steps from MOSFET scheme are not followed.



(a) **(b)**

Figure 2.13: (a) Schematic of a SOI based SET operating at 300 K. (b) $I_D - V_G$ and $G_M - V_G$ characteristics at 300 K. Figure from [Zhua 98].

featuring a channel connecting source, drain regions with a gate on top of the channel. The active area patterning was done using e-beam lithography and reactive ion etching (RIE). The channel was a nanowire with an island in between (slightly larger than the wire). Constrictions were defined in the nanowire to create the island and the constrictions were expected to act as tunnel barriers (owing to higher potential from reduced width). Figure 2.13b shows the $I_D - V_G$ and transconductance of the SET. The step like behavior of $I_D - V_G$ indicates single electron charging phenomena of the channel

island. The peaks in transconductance are an additional confirmation of the same. The nonlinear transport measurements CB plot also show some coulomb diamonds and the authors reported optimistic addition energy values of 110 to 130 meV. Though it was a nice demonstration of SET at room temperature, a lot was to be improved in the $I-V$ characteristics to make SET based circuits feasible.

Another method of fabrication named PADOX (PAttern Dependent OXidation) has been pursued by researchers from Japan (NTT, Tokyo Univ. etc)[Ono 00, Taka 03] over the last decade to obtain high charging energy in CMOS SETs. The key part of the fabrication process is the channel formation. The process relies on difference in oxidation rate of the nanowire channel (∼30 nm) from that of wider source/drain areas. Nanowire channel fabrication is similar to one previously mentioned (e-beam lithography, RIE on SOI) except that channel diameter is further reduced from the lithography defined value by oxidizing the silicon for long durations. In this process nanowire channel undergoes what is popularly known as 'self-limited oxidation'[Liu 93]. As the oxide layer grows on the nanowire, a stress builds up. Since the oxidation for

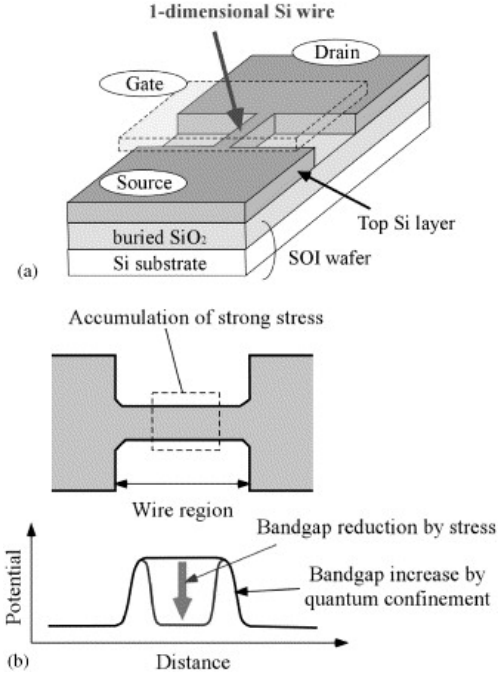


Figure 2.14: (a) Schematic of the SET made by PADOX process on SOI.[Taka 03](b) Explanation self aligned island and tunnel barrier formation in PADOX process.

nanowire is from all sides, a compressive stress builds up that eventually saturates

oxidation. Hence it is self-limiting or saturating process. However, this effect doesn't occur for the wide planar source/drain regions. The accumulated stress in nanowire possibly leads to change in bandgap (compared to S/D regions) creating a potential well. Thus the island and self aligned tunnel barriers are formed in the process. Schematic in figure 2.14 explains this effect.

Utilizing similar process integration scheme, further progress was made recently by Shin et al [Shin 10]. Active area was patterned as silicon fin and then a section of it was subjected to 'self-limited oxidation'. Rest of the fin was masked by spacers. This reduced the oxidized part to a nanowire of 2-5 nm diameter. Schematic of the device is shown in figure 2.15a. The island is formed in an extremely small nanowire of diameter 2 nm (TEM of the nanowire cross section: Fig. 2.15b). Clear Coulomb oscillations are observed in the $I_D - V_G$ curves of the device at room temperature (Fig. 2.15c). Corresponding Coulomb diamonds for the device are shown in figure 2.15d. From the diamonds, the charging energy is estimated to be 380 meV.

Though this method is useful to create stable, charge-fluctuation immune SET, room temperature operation with clear oscillations and high peak-valley-current-ratio (PVCR) has been limited. Also, as it relies on oxide induced stress for SET formation it would require very thick gate oxide layer. This would be a major challenge for cointegration of SET with scaled MOSFETs as they require very thin gate oxide layer. There are also quite a few results showing very high PVCR especially from Prof. Hiramoto group at Tokyo University [Ishi 96, Sait 01, Sait 04]. The process scheme involves island and tunnel barrier formation in a nanowire channel. They are formed similar to the work of Chou et al., except instead of intentionally patterning constrictions, the nanowire wet etching process is so designed as to create width fluctuations that create island and constrictions [Ishi 96]. The $I_D - V_G$ characteristics of a SET fabricated with this process scheme [Sait 04] is shown in figure 2.16.

However, the major challenge in this process are the extremely low current of the Coulomb peaks (few pA). Besides, the nanowire is realized by e-beam lithography and special isotropic etching process that induces roughness in channel edges Also, the gate stack is SiO_2/Poly-Si. Therefore it would be an issue to cointegrate with FET on CMOS technology. Despite this challenge this method has led to many demonstrations of room temperature operating SET and combined SET-FET circuits with large number of functionalities [Sait 03, Sait 04].

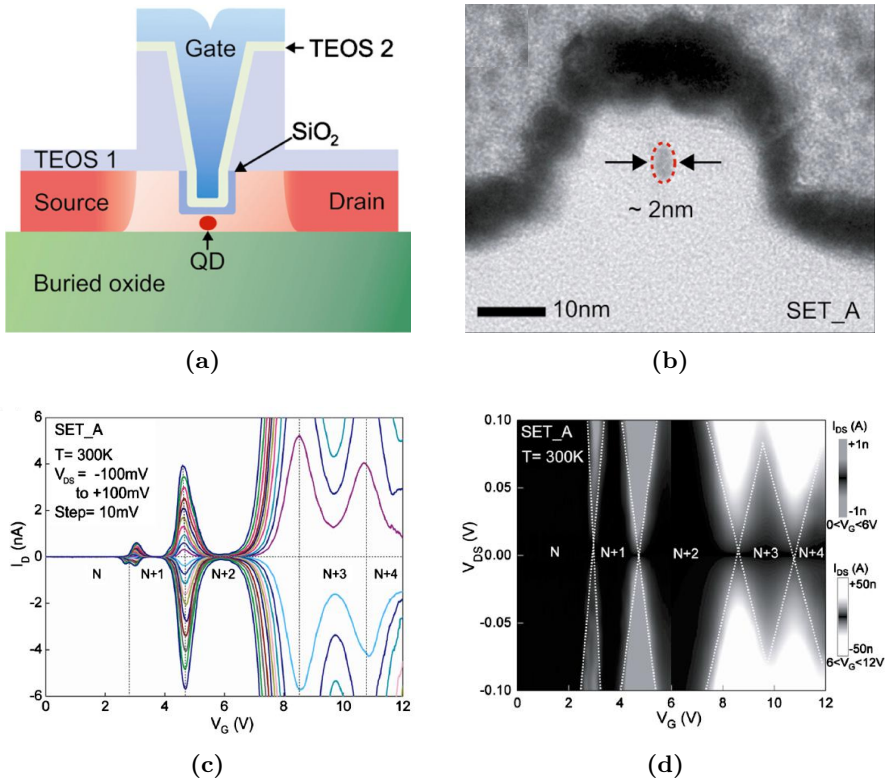


Figure 2.15: (a) Schematic of SET operating at 300 K fabricated from modified finFET channel [Shin 10]. (b) TEM of the cross section of the channel showing nanowire with 2 nm diameter. (c) $I_D - V_G$ characteristics at 300 K. (d) Coulomb diamond plot of the device at 300 K.

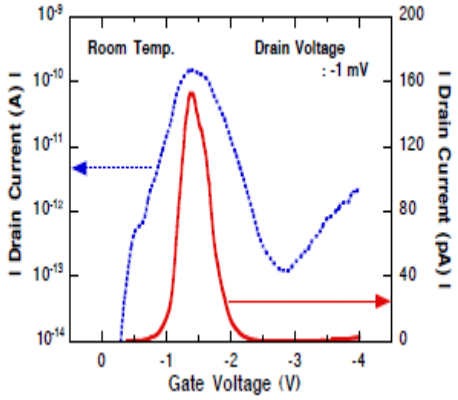


Figure 2.16: $I_D - V_G$ characteristics of SET formed from Si nanowire with width fluctuations [Sait 04]. The SET shows high PVCR oscillation, but with low current due to highly resistive barriers.

3

Room Temperature (RT)-SET Integration on CMOS

For room temperature operation the SET fabrication technology has to be capable of realizing island or channel of nearly 5 nm dimensions and should be CMOS compatible. As seen in the last chapter, most of the Si based RT-SET integration scheme are a modification of SOI-MOSFET integration scheme. In this chapter, we describe our approach to CMOS RT-SET. Our integration scheme involves no modification to SOI-MOSFET integration scheme. In fact we develop an integration scheme common for both RT-SET and end-of-roadmap (8 nm node) trigate nanowire MOSFETs. Critical process steps that enable realizing 5 nm width nanowires are detailed. We then show the electrical characteristics of the devices fabricated. We show both excellent RT-SETs and end-of-roadmap nanowire MOSFETs. The physical mechanisms that lead to RT-SET observation in our devices are then discussed in detail. We also discuss low temperature transport properties in these device to gain deeper insights. The low temperature behavior of RT-SETs is also compared with ultrascaled nanowire MOSFETs.

3.1 CMOS-SET Integration Scheme: Towards a MOSSET

We have pointed out in the preceding sections on how important it is to have a SET fabrication process (or integration scheme) as close to conventional CMOS integration as possible. We reiterate again that the benefits are multi-fold. The biggest benefit obviously is the technological maturity and economics of scale of the CMOS technology.

If SET integration scheme fits well with MOSFET integration i.e. if we can achieve SET-FET 'cointegration' then all the forces driving the FET based VLSI systems would also drive the SET based circuits. One can thus make SET as a 'mainstream' device on the same footing as a MOSFET! Also, same integration scheme would enable seamless cointegration of SET-FET circuits for LSI or VLSI systems. This would add new functional circuits hitherto absent in CMOS portfolio [Wagt 99]. With these motivations we make an effort to develop an integration scheme that would enable us to realize a SET in CMOS technology, what we would like to call a *MOSSET*.

Besides the general advantages that a 'MOSSET' scheme would provide, there is also another strong technological motivation for our approach. As we all know, the continuous downscaling of MOSFET dimensions have brought us into a nano-MOSFET era. Scaling has become more challenging than ever before. Significant material and structural changes are being introduced at every new technological node to meet these challenges. As described in the general introduction (chapter 1), multigate architecture is being pursued as a possible solution to the end-of-roadmap node (8 nm). The scaling rules, for instance, for trigate MOSFET require $L_G > 3R\,or\,(3W/2)$ [Yu 08]. Therefore we need to have a nanowire channel with width nearly 5 nm for 8 nm node gate length. Now, comparing this requirement with that for RT-SET we see that they are the same. For better operation RT-SET could have even smaller nanowire. So in terms of channel dimensions the same technological developments are required for both RT-SET and end-of-roadmap nanowire FET. In fact one can look at SET as the 'next scaled node' of 8 nm node nanowire FET. Thus we have actually put the RT-SET on the CMOS roadmap itself! (just *Beyond Moore's limit*). It gives all the more reason to develop MOSSET integration scheme as it would be a synergic development for scaled nanowire MOSFET as well.

In the following sections we discuss the main technological challenges that have to be addressed in order to develop a reliable MOSSET integration scheme.

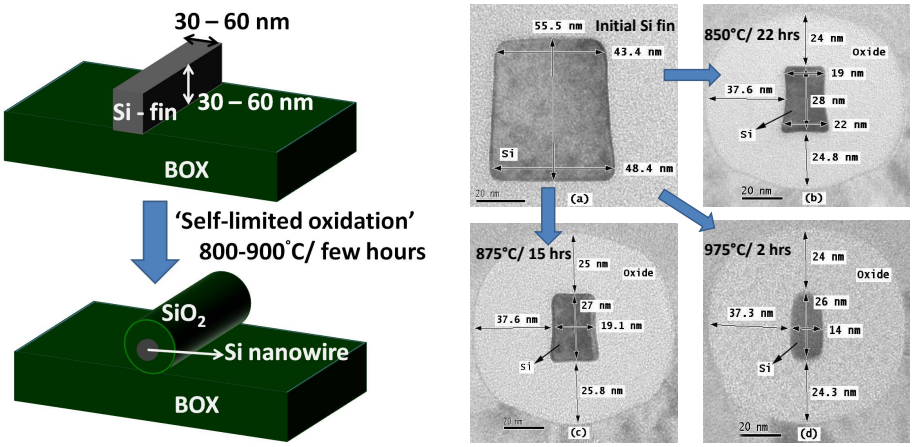
3.1.1 Challenges for Sub-10 nm Width Nanowire Channel

Both the RT-MOSSET and end-of-roadmap nanowire MOSFET require a nanowire channel with diameter or width around 5 nm. Fabrication of such an ultrascaled nanowire channel under current CMOS process is an immense technological challenge. The major bottleneck is the lithography. Optical lithography, which is the industry

standard for lithography in CMOS integration scheme, can at best provide a pattern of critical dimension (CD) = 50 nm [Niko]. This too, is only possible with 193 nm DUV (Deep-UV) source and projection lens system (generally known as 'projection lithography'). The widely employed lithography on lab-scale for obtaining sub-100 nm width patterns is the e-beam lithography [Wied 10]. As electrons have smaller wavelength, the diffraction limit is smaller. This enables one to obtain patterns much smaller than that possible through optical lithography. All the previous works that realized excellent RT-SET employed e-beam lithography for nanowire pattern definition. However, owing to very small throughput (number of wafers per hour) e-beam lithography is not a feasible option for large volume CMOS manufacturing. Besides, even with e-beam lithography direct patterning of sub-10 nm nanowires is extremely difficult. In future, EUV (Extreme-UV, wavelength = 13.5 nm) lithography may enable much smaller patterns. But until now this technology is not mature enough to be adapted for mainstream CMOS processing. Therefore, innovative methods are required to realize sub-10 nm nanowires with current DUV optical lithography alone.

Many efforts have been done previously to realize sub-10 nm diameter nanowire channels [Yeo 06, Sing 06, Song 12, Bang 09, Tach 10]. Some of these employ e-beam lithography while others employ optical lithography. However the main process that leads to sub-10 nm nanowires in most of these works is not greatly dependent on the lithography used. Hence, it can well be done with optical lithography. Also, this has led to the only demonstration of RT-SET fabricated through optical lithography alone [Sun 11b].

We will now describe two processes that have been widely used and are most reliable (to the best of our knowledge) for forming sub-10 nm nanowires. The first one is the 'self-limiting oxidation' method which has been mentioned in the last chapter. The process scheme involves patterning of active area (by e-beam or optical lithography) in the form of a silicon fin which is generally 30-60 nm wide and nearly of the same height (Si thickness). It is then subjected to long oxidation, typically few minutes to few hours depending on the initial nanowire size. As the nanowire gets oxidized, its size gets reduced. However, after certain time the oxide growth saturates as oxygen atoms can no longer reach the silicon atoms in the nanowire which is now covered with a thick oxide layer. This oxygen diffusion limit is caused by the stress that has built up in the oxide



(a) **(b)**

Figure 3.1: (a) Schematic of self-limited oxidation process. (b) Cross section TEM images of initial Si fin and subsequent nanowires formed by self-limited oxidation process for different oxidation time and temperatures (mentioned on each figure). Top left figure corresponds to initial Si fin. Figure taken from ref [Ma 09]

due to its growth from all sides [Ma 09]. Figure 3.1a shows the schematic of the 'self-limited oxidation' process for fabricating Si nanowires. Figure 3.1b shows cross-section TEM images of nanowire formed by this process(figure from [Ma 09]) beginning with a nearly 50 nm×50 nm Si fin and performing dry oxidation at different temperatures and different times. However, in this method the limiting size of the nanowire is highly sensitive to initial fin patterns [Dupr 08] and fluctuations in the width may lead to complete oxidation in narrower sections and breaks in the wire. Also when sub-10 nm nanowires are made this way it becomes important to keep the oxide shell intact in order to protect the wire during further processing (gate deposition, spacer patterning etc.). Removal of oxide shell results in a hanging wire of very small diameter which may be broken during gate deposition or etching. Besides, complete removal of oxide would force one to have Gate-All-Around (GAA) geometry. This geometry poses one notorious problem of 'poly stringers'[1] below the nanowire when gates shorter than the wire length are etched. During poly-Si plasma etching suspended nanowire masks poly-Si below it and leads to unetched gate stringers below non-gated regions on the nanowire. So one has to resort to more complex gate integration schemes like 'damascene method'

[1]Poly stringer is the residual poly-Si (after gate etch) below nanowire in areas not covered by the gate.

to realize ultra-short gate lengths [Yeo 06].

Another method for realizing sub-10 nm nanowires was demonstrated recently by IBM Watson research centre [Bang 09], where nanowire dimensions down to 3 nm were reliably obtained by e-beam patterning, resist trimming, hydrogen annealing and small oxidation (about 5-6 nm). The process scheme involves patterning of active area in the form of a silicon fin which is about 30 nm wide and nearly of the same height (Si thickness). It is then subjected to annealing under hydrogen gas ambient. This hydrogen annealing serves two purposes. Firstly, it 'rounds' the nanowire and reduces surface roughness introduced during patterning [Dorn 07] (litho and etch). Secondly, it moves the silicon atoms around [Sudo 04] which leads to diffusion of Si atoms from nanowire to S/D pads. Thus it reduces the nanowire width (this process has been termed 'maskless thinning' [Bang 09]). In this way nanowire width may be reduced to about 10-15 nm. Thereafter it is subjected to high temperature oxidation, which can further reduce the nanowire width down to 3 nm. The oxide may be etched and high-k gate oxide may be deposited subsequently. The process sequence described above is shown in figure 3.2. Nanowires down to 3 nm width are reliably obtained through this method. Figure 3.3 shows the process of 'maskless thinning' of NWs by hydrogen annealing.

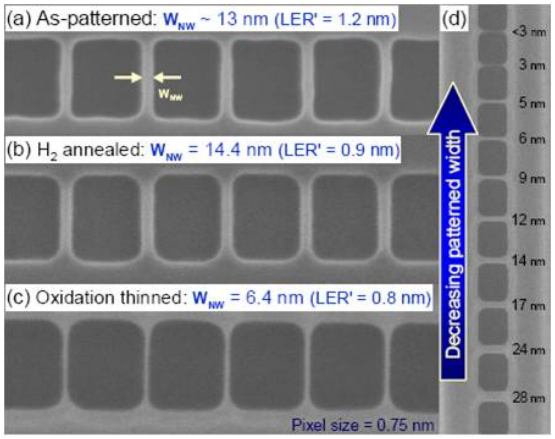


Figure 3.2: Process sequence for realizing sub-10 nm NW (Figure from [Bang 09]). (a) NWs with S/D pads on SOI after patterning (lithography and RIE). (b) Hydrogen annealing to smooth the NWs. (c) Sub-10 nm NWs by high temperature oxidation. (d) NWs with various widths (down to 3 nm) reliably formed by patterning, H_2 anneal and oxidation.

This method seems more reliable for producing NWs with less variability. Also, it

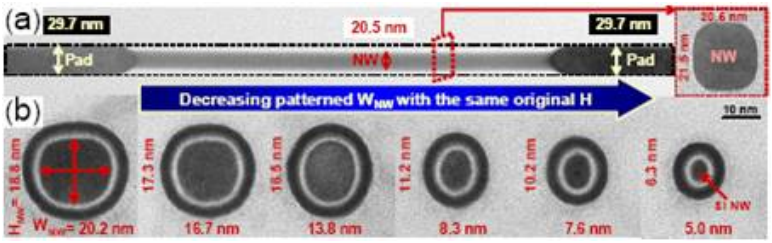


Figure 3.3: Hydrogen annealing of NWs for maskless thinning and reshaping (Figure from [Bang 09]). (a) Nanowire is thinned while S/D pads retain their thickness due Si migration from NW to pads. (b) Effect H_2 anneal on initial NW width. Smaller width leads more Si migration (due highly curved surface) and hence more reduction in width during the process.

enables easy integration of high-k/metal gate stack with sub-10 nm NWs. However, it still leads to GAA geometry requiring highly optimized process for gate etching (to avoid stringers). Also, for very small NWs (sub-15 nm width) hydrogen annealing may lead to fragmentation (due to Si agglomeration) [Dupr 08]. Hence very tight control on initial NW width and H_2 anneal process parameters are required.

3.1.2 Optimal tunnel barriers

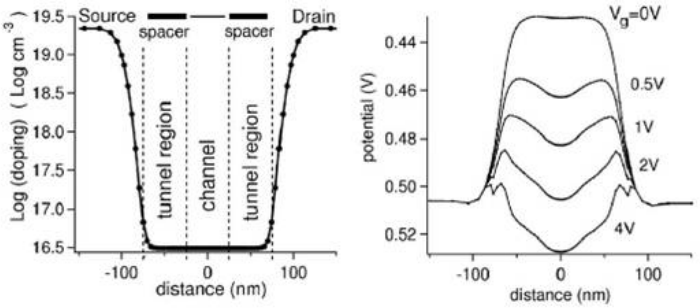
Besides the requirement of sub-10 nm diameter/width nanowires, MOSSET also needs optimal tunnel barriers to confine electrons in channel. Formation of optimal tunnel barriers is also a major issue. The tunnel barriers should not be too high and wide (leads to reduction in current) and not too low (thermal activation of electrons lifts CB). Also, they should have small capacitance as it has been seen that larger C_S and C_D lead to reduced charging energy. In most of the Si based RT-SETs the origin of tunnel barriers is not well understood [Sun 11a, Sun 11b]. In most of these RT-SETs island and tunnel barriers are formed either by potential fluctuations induced due to the surface roughness introduced during channel etching and oxidation or due to disorder in intrinsic channel. It is evident in low temperature characteristics of such devices where coulomb oscillations become non periodic due to multiple island formation. However, two methods of forming well-controlled, reliable tunnel barriers in CMOS compatible SETs have been proposed in literature. We will briefly discuss them in following paragraphs.

SET fabricated on CMOS platform resembles an ultra scaled nanowire MOSFET, with the only difference being the 'access'. The 'access region' is the souce/drain to

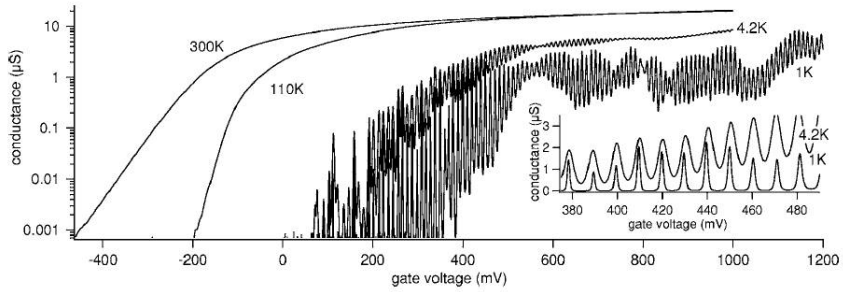
channel junction. In the case of MOSFET it is a simple p-n junction and is required to have as less resistance as possible. In the case of SET this junction should be a 'tunnel junction' and should have a resistance of at least 26 kΩ (with RT-SETs typically having around 1 MΩ [Sait 03, Sun 11b]). Typically in a MOSFET the highly doped (HDD- high dose doping) source/drain regions are connected to channel through a moderately doped extension (called LDD- low dose doping) below the spacers. This is done to reduce the access resistance and increase the current levels in the FET. Our research group at CEA-INAC and LETI demonstrated a simple and well-controlled SET by very simple modification of doping in access region of FET [Hofh 06]. The LDD region in MOSFET was removed, thereby leaving nearly intrinsic silicon below the spacers. This doping modulation leads to increase of potential below the spacers, thus creating self aligned tunnel barriers. The schematic in figure 3.4a shows how the island and tunnel barriers are formed in a self-aligned manner on application of gate voltage in this 'doping modulation SET'. However, these barriers are 'disordered insulators' acting as tunnel barriers [Hofh 07] since Coulomb oscillations are also observed when the spacers are as thick as 40 nm, which otherwise is too long for electrons to tunnel through.

Figure 3.4b shows typical electrical characteristics of such a doping modulated SET. Since the integration scheme is very close to standard MOSFET fabrication, the reliability of these SETs is quite good. However, highest charging energies obtained till now has been only about 20-25 meV [Pier 11] which is quite far from the room temperature requirement($\sim$100meV). There may be multiple reasons to this and it will be analyzed later in this chapter.

The other scheme of controlled tunnel barrier formation in CMOS compatible Si SETs was demonstrated in PADOX based SET fabrication described in detail in the last chapter. The authors have claimed that the barriers in the SET are formed in self aligned manner when the channel is created. They explained it on the basis of the stress generated during oxidation. This stress leads to reduction in bandgap in the channel region. As a result the bottom of conduction band is at lower level compared to that in source/drain pads. This creates a potential well in the channel. However they have made an assumption that this bandgap lowering is effective only deep in the channel where diameter is lowest and not in the region near source/drain pads where wire widens before merging into pads. So the whole explanation for tunnel barrier formation rests on this assumption!



(a)



(b)

Figure 3.4: (a) Simulated doping concentration and channel potential profile for doping modulation SET [Hofh 06] (b) Typical Conductance$-V_G$ characteristics of doping modulation SET. Figure from ref [Hofh 06].

3.2 Our MOSSET Integration Scheme

In the last section, we have looked at different integration schemes for Si nanowires in CMOS process. As mentioned before though 'self-limited' oxidation and 'maskless thinning' schemes enable sub-10 nm NWs, they force one to use GAA geometry for NWs if one intends to have high-k/metal gate stack. Therefore, due to the additional complexity involved in gate patterning steps, we have decided to use 'trigate' geometry. This geometry gives equally competitive electrostatic control over channel (as compared to GAA) and has added advantage of simple integration scheme. We use SOI substrate for our MOSSET and NW-MOSFET integration. Naturally, using 'mesa' isolation on SOI enables trigate geometry without any complex integration scheme.

The full integration scheme developed by us for MOSSET and NW-MOSFETs on SOI is shown in figure 3.5. Starting from a SOI substrate (T_{Si}=12 nm), NWs are patterned using 193 nm DUV lithography. Resist trimming is performed during etching to reach NW widths down to 5 nm. We have two splits in NW width, W = 20 nm and

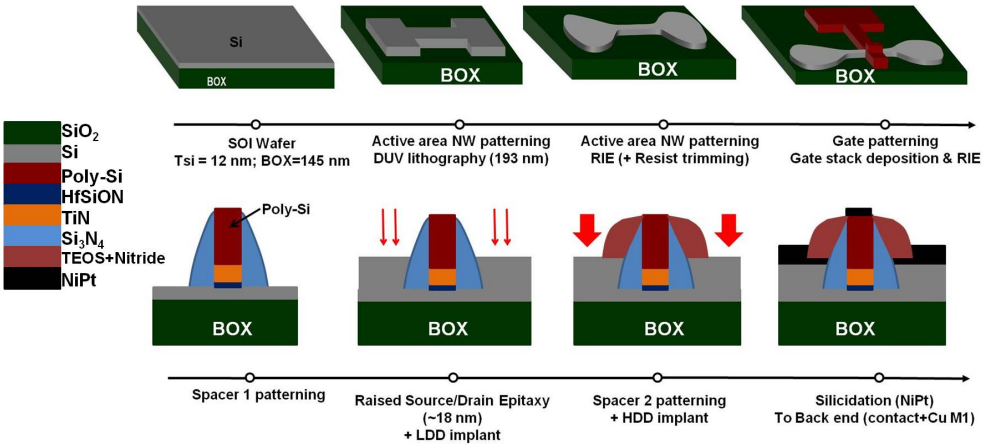


Figure 3.5: Schematic of the MOSSET/NW-MOSFET integration scheme developed by us. Only the front-end-of-line (FEOL) process steps are shown. The back-end-of-line (BEOL) involves standard CMOS process steps with Cu back-end. [Desh 12]

W = 5-7 nm. This is the most important part of the integration scheme that enables sub-10 nm NWs. The details of this process will be discussed in the next section. As we aim to develop a common integration scheme for both MOSSET and NW-MOSFET for end-of-roadmap node we use metallic gate and high-k dielectric as gate oxide. Therefore high-k/metal gate stack comprising of 2.3 nm HfSiON, 5 nm ALD TiN and 50 nm poly Si is then deposited. The pre-deposition cleaning is adapted to form an interfacial SiO_2 layer. Now gate down to 20 nm is patterned, again with DUV lithography followed by resist trimming and RIE. We use mesa isolation, so the gate covers the nanowire on three sides making it 'trigate' geometry. Offset nitride spacers are then formed; CD Spacer 1 (shown in blue, Fig. 3.5) = 25 nm for 5-7 nm width NW and CD Spacer 1 = 10 nm for 20 nm wide NW. Silicon epitaxy is then performed on source/drain areas to obtain raised source/drain. LDD doping is then performed. Now second offset spacer consisting of TEOS liner and nitride spacer is patterned. It is then followed by HDD doping to define source/drain and silicidation (with formation of NiPt silicide) for lower contact resistance. Tungsten contact and standard Cu back-end follows thereafter.

3.2.1 Formation of Sub-10 nm Width Nanowires

The most important part of the MOSSET/NW-MOSFET integration is the active area patterning i.e. sub-10 nm width nanowire formation. We achieve this with 193 nm DUV lithography (DUV stepper tool) and resist trimming. The minimum pattern

width obtained after lithography is about 80 nm. The active stack used consisted of undoped Si, SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer patterned using 193 nm ArF resist. The thickness of the photoresist is adapted to have proper aspect ratio at the end of trimming. The active zone (i.e. nanowire feature) etching is carried out using the trimmed resist/BARC as a mask. Obviously, the final line-width of nanowires is determined mainly by the amount of trimmed resist.

Figure 3.6 shows the process sequence used for NW patterning through resist trimming. First of all, HBr plasma curing process was performed in order to harden the 193 nm ArF resist for better etching resistance. Then, the BARC opening is done using CF_4 chemistry. This chemistry has been used in order to ensure vertical resist/BARC profile and correct line-width roughness. Moreover, as this sequence consumes a lot of photoresist, the thickness of the BARC layer is well adapted to minimize the resist budget during the process. Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire structures as small as 5 nm of width using the HBr/O_2 plasma.

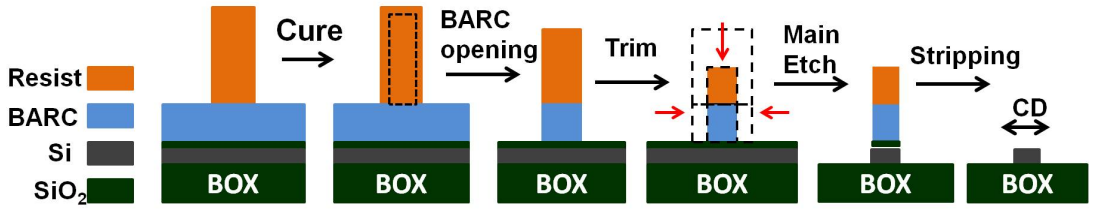


Figure 3.6: The process sequence used for NW patterning through resist trimming.

Through this process of resist trimming NWs of different width can be patterned at the same time. Depending on the initial pattern width after resist development, different widths can be obtained after trimming and etching. The resist width reduction during trimming is well controlled for same kind of patterns. Hence we can obtained nearly same width nanowires all across the 300 mm wafer after etching. Figure 3.7 shows different nanowire patterns: After etching and after gate patterning. We had both isolated nanowires and parallel nanowire arrays (50 to 100 NWs). Both of these patterns can be reduced to around 10 nm width through resist trimming. There were also devices with very wide active areas (planar MOSFETs) as reference. It can be seen that width reduction (for the same trimming time) is different for different patterns

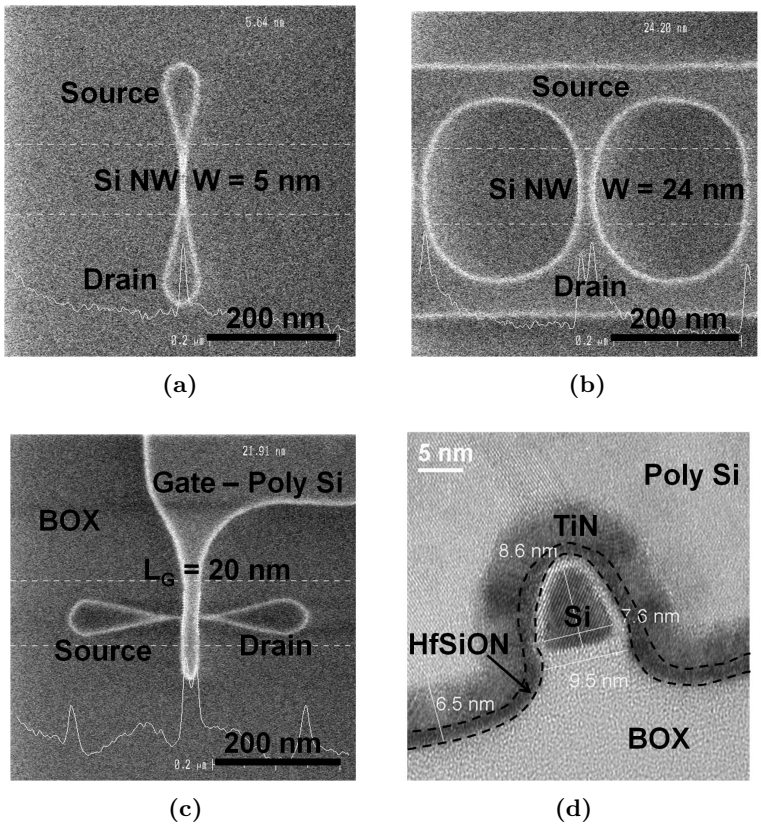


Figure 3.7: Top view SEM images of NWs after etching (All NWs had nearly same width after lithography.) (a) Single nanowire (W=5 nm) (b) Nanowire array (W = 24 nm) (c) Single nanowire with gate patterned (L_G = 20 nm. (d) Cross section TEM of a 7.5 nm wide nanowire.

(figure 3.7). This is because the resist width reduction during trimming depends on the local density of patterns. In case, similar NW width is required for both isolated NW and NW arrays then the trimming parameters (time, chemistry etc.) have to be optimized properly to achieve same dimensions. However, one can also benefit from this difference in trimming rates in the following way. MOSSET requires single NW and NW-MOSFETs need multiple nanowires for high current drive. So they can be realized simultaneously by making MOSSET from isolated NWs and NW-MOSFETs from NW arrays. Also, it has been observed (in our current process) that the resist trimming rate is higher for isolated nanowires. This is also beneficial as for the same trimming time one can obtain smaller width isolated NWs and larger width NW arrays. This matches perfectly with channel width requirements of MOSSET and NW-MOSFET

respectively.

3.3 Electrical Characterization

3.3.1 Room Temperature Characteristics

In this section we present electrical characterization of NW devices. In total 13 wafers of 300 mm diameter were characterized on standard I-V/C-V test probe stations (Cascade Microtech) and the I-V measurement was done through standard semiconductor parameter analyzer equipments. On all the wafers, 18 dies were measured covering all the quadrants of the wafer. The dies chosen for electrical characterization were the same dies on which in-line CD-SEM measurements were carried out after active area patterning (litho and etch), gate patterning (litho and etch), spacer 1 patterning and epitaxy. Since there is a dispersion in the width of nanowires across the wafer, characterizing the dies whose width measurements are available eases interpretation of the measurements.

3.3.1.1 Scaled NW-MOSFET Characteristics: W = 20 nm and 5-7 nm

As mentioned before, we have two splits in width for the nanowire. This refers to the width of isolated single nanowires and not to nanowire arrays[1]. The two width splits that we have on our batch are: a) Average W = 20 nm (3σ ~5 nm)[2] and b) Average W = 7 nm (3σ ~4 nm). The values mentioned here are top view measurements performed with CD-SEM, after etching the nanowires (Details of measurement statistics are given in Appendix A.1). It is to be noted that the CD-SEM used for width measurements does not have enough resolution to clearly resolve nanowires with width less than 15 nm. The best resolution is about 2 nm. So, for example, values mentioned between 5 nm and 7 nm are indicative of relative size and should not be considered as exact width of NWs. Accurate CD measurements for sub-10 nm patterns is still a topic of research in metrology.

Since the NW-MOSFET have better electrostatic integrity as compared to planar MOSFETs, they can be scaled to much lower gate length than planar ones. In order

[1] We will be mostly discussing about characteristics of single isolated NW rather than arrays as these are the ones that will be used to realize SETs.

[2] σ - standard deviation

to establish the scaling of our NW-MOSFETs to end-of-roadmap requirements, we first show short channel effect (SCE) control. Fig. 3.8a and 3.8b show SCE control down to L_G = 20 nm for NMOS with different NW widths. For gate length, L_G = 20 nm, drain induced barrier lowering (DIBL) and subthreshold swing (SS) are 30 mV/V and 72 mV/dec respectively for NW width = 20 nm. For the same L_G on reducing width to 7 nm, DIBL and SS are reduced to 12 mV/V and 62 mV/V respectively, showing excellent SCE control with width reduction. The $I_D - V_G$ plots

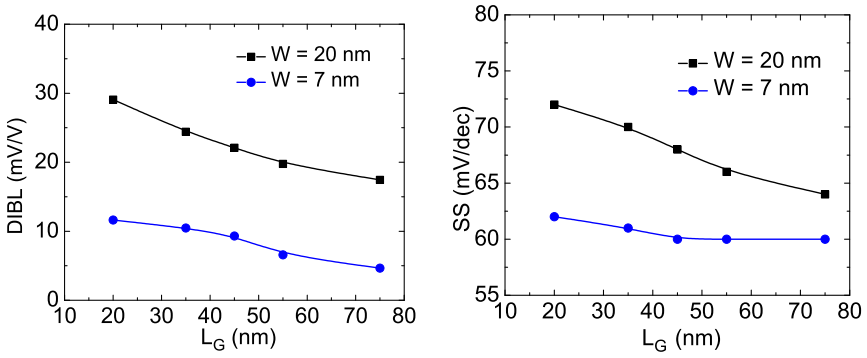


Figure 3.8: SCE control by width scaling in Trigate NW-NMOSFETs. (a) DIBL vs. L_G for different width NWs down to L_G=20 nm. Drastic improvement in DIBL for L_G=20 nm from 30 mV/V for W=20 nm to 12 mV/V for W=7 nm. (b) SS vs. L_G for different width NWs. Improvement for L_G=20 nm, from 72 mV/dec for W=20 nm to 62 mV/dec for W=7 nm.

for L_G=20 nm NMOSFETs with NW width=20 nm and 7 nm are shown in Fig. 3.9a and Fig. 3.9b respectively. Though SCE control is already quite good for W = 20 nm nanowire, it is further improved on scaling width down to 7 nm. However, it can be seen that the ON state current of 7 nm nanowire is less as compared to 20 nm nanowire. This is due to larger CD of spacer 1 for 7 nm nanowires, which increases the access resistance.

Now we look at the PMOSFET performance. Figure 3.10a and 3.10b shows the DIBL vs. L_G and SS vs. L_G down to L_G = 20 nm for PMOSFETs. It is seen that W = 20 nm nanowires shows expected trend in both DIBL and SS with L_G, i.e. DIBL and SS increase with decreasing gate length. However, PMOS with nanowire width = 7 nm do not show clear trend in DIBL and SS with L_G and also no significant improvement as compared to 20 nm width nanowires. NW-PMOSFETs with W =

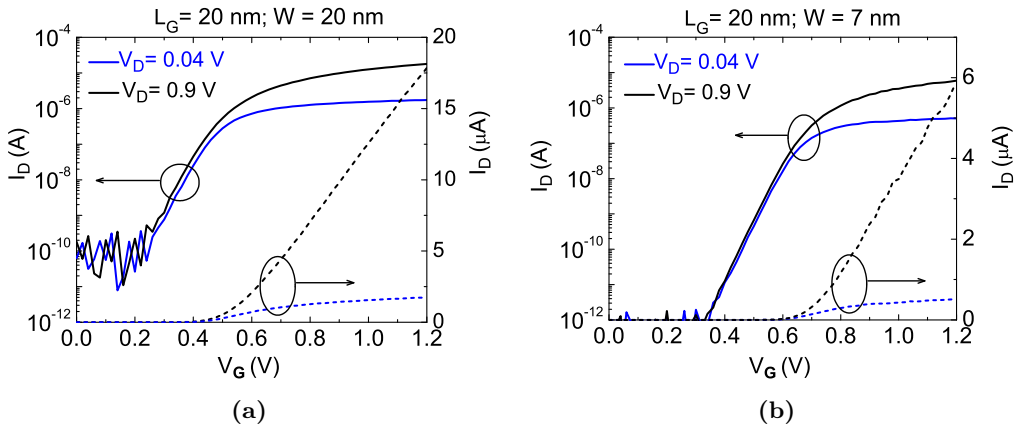


Figure 3.9: (a) and (b) $I_D - V_G$ at V_D = 0.04 V and 0.9 V for L_G = 20 nm with W = 20 nm and W = 7 nm respectively. Solid lines for I_D in log scale and dashed lines for I_D in linear scale.

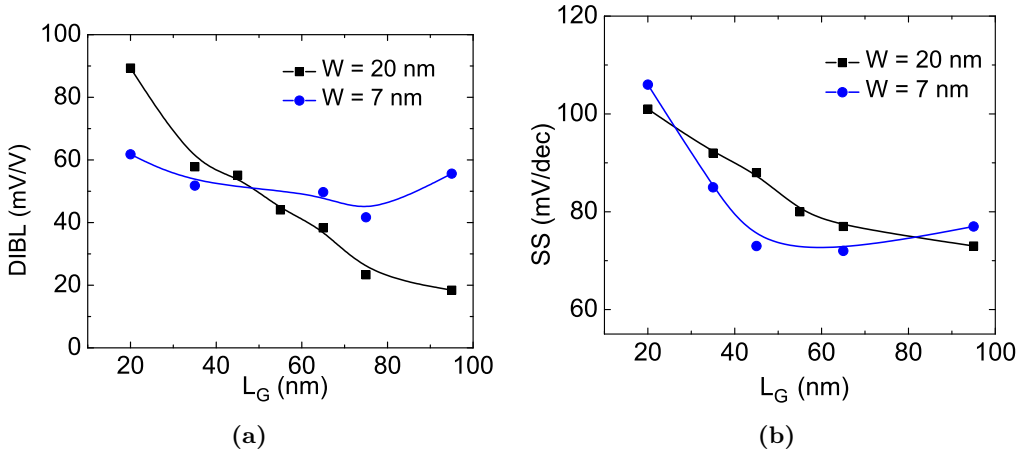


Figure 3.10: SCE in Trigate NW-PMOSFETs. (a) DIBL vs. L_G for different width NWs down to L_G=20 nm. (b) SS vs. L_G for different width NWs.

7 nm have higher DIBL as compared to 20 nm width nanowires. This behavior was verified with large statistics (measurements on around 300 devices on different wafers) and the same behavior has been observed. Moreover, there is also increased dispersion in values of DIBL and SS for PMOS as compared to NMOS for nanowires with W = 7 nm. It is not yet clear if the origin of degradation is due to a problem with some process step or intrinsic to NW-PMOSFETs. This is an area of further investigation.

The $I_D - V_G$ curves for PMOS devices with L_G = 20 nm are shown in figure 3.11a

and 3.11b respectively. Degraded gate control on 7 nm nanowire devices is clearly visible.

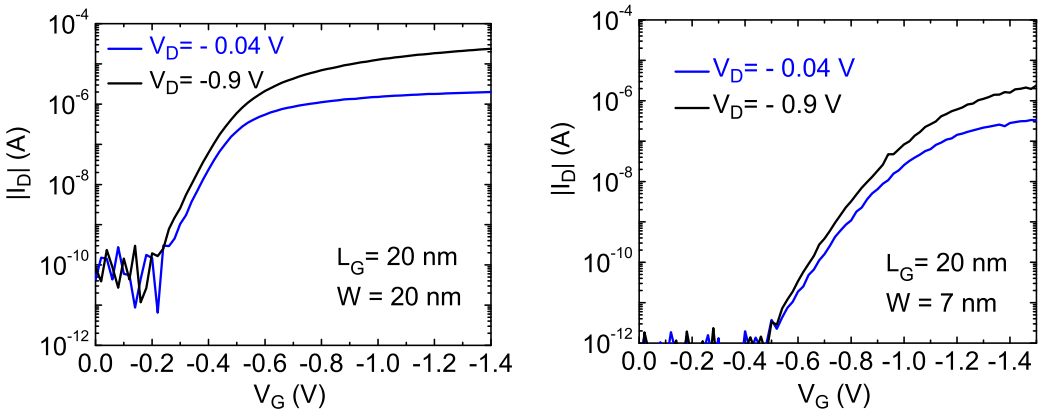


Figure 3.11: (a) and (b) $I_D - V_G$ for PMOS at V_D = -0.04 V and -0.9 V for L_G = 20 nm with W = 20 nm and W = 7 nm respectively.

3.3.1.2 Room Temperature MOSSET in 5-7 nm Width Nanowire: FET to SET Transition at 300 K

In this section we present room temperature operating SET by scaling the nanowire width to about 5 nm (or below). All the subsequent measurements are performed at 300 K unless specified. Besides having excellent short channel effect control in NWs with W = 7 nm, we have observed a variability leading to peculiar characteristics in some devices. As shown in section 3.2, there is a dispersion in nanowire width from 5-7 nm after etching. Taking advantage of this, we can study the scaling of nanowire down to 5 nm width. On these nanowires, i.e. when W = 5-7 nm, we observe a complete change in transport characteristics. Fig. 3.12a shows the $I_D - V_G$ characteristics of a NMOS with W = 5 nm (we call it device A) with classical FET behavior. However, another device (device B) with same nominal dimensions shows weak oscillations in the drain current at 300 K (Fig. 3.12b). These oscillations are due to single electron charging or 'Coulomb blockade' phenomenon. Therefore, device B is operating as a SET, albeit with very weak oscillations. Thus, even with a the same nominal dimensions, we observed two different transport mechanisms in these 5 nm width nanowires. It could in fact be considered as a FET to SET transition.

We now try to explain the origin of this transition. As the nanowire width is very small, its potential is very sensitive to disorder. Since we have fabricated nanowires with RIE, some disorder (surface roughness for instance) introduced in the NW. This leads to a disorder potential in the channel (Fig. 3.12b schematic). Such a disorder potential creates confinement of electrons leading to island formation in the NW. In case of nanowires with surface roughness, island formation due to disorder potential has also been demonstrated in the simulation works [Lher 08, Sviz 07]. These islands show Coulomb blockade phenomena and the transport in such NWs becomes markedly different from the classical MOSFET case. Thus we reason that the FET to SET transition in our nanowires and the corresponding variability is due to channel potential profile variability introduced by disorder, with FET case having smooth channel potential and SET case having disorder potential (for instance due to line edge roughness (LER) [Lher 08, Sait 03]).

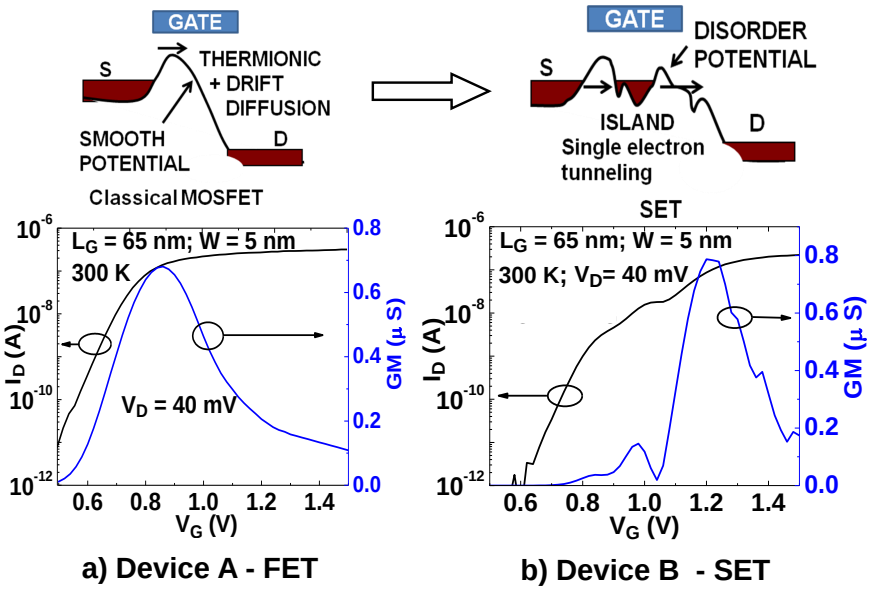


Figure 3.12: I_D-V$_G$ and transconductance (GM)-V_G plot for two NMOS (device A and B) with nominally same dimensions. Transition from MOSFET to SET is observed due to channel potential variation (schematic above graphs) (a) Device A works as classical MOSFET. (b) Oscillations observed in I_D and GM of device B. Peaks marked by arrows (separation = 160 mV). Device B behaves as SET.

Fig. 3.13 shows another device (device C), a PMOS exhibiting strong Coulomb

oscillations in the drain current. The device is in fact operating as a very good Single Hole Transistor. Good peak to valley ratio is observed with quasi periodic oscillations. Fig. 3.14 shows the 'Coulomb Diamond' (2D color plot of I_D with V_G and V_D) for device

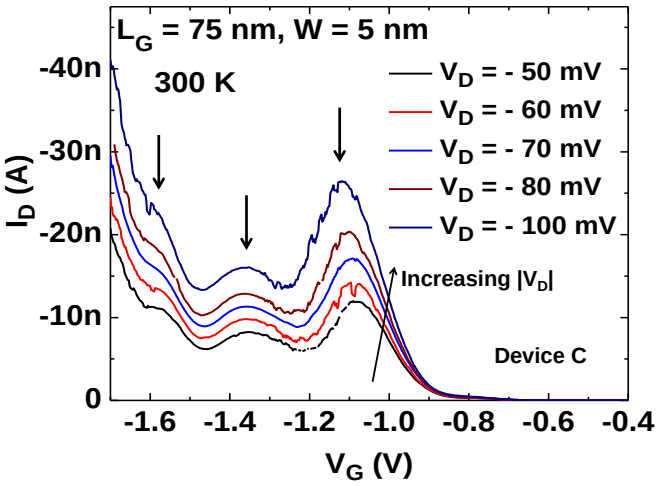


Figure 3.13: $I_D - V_G$ characteristics of a PMOS SHT (Single Hole Transistor) at 300 K - device C. Three peaks corresponding to single electron charging are observed. V_G period of the oscillations is about 280 mV giving gate capacitance C_G=0.57 aF.

C. Slopes of the diamond (shown in figure) give C_S and C_D, which are 0.85 aF and 0.48 aF respectively. We had discussed in the last chapter that for small semiconducting islands, the single particle level separation is high (sizable fraction of charging energy). So separation between current peaks includes gate capacitance and level separation and is equal to 0.57 aF (Device C). This yields a total capacitance of the island ∼2 aF. Therefore the addition energy given by $\frac{e^2}{C_\Sigma} + \Delta_1$ (cf. section 2.1) is estimated to be ∼85 meV. Small capacitance of the island results in high charging energy that is greater than thermal energy at room temperature (25 meV) and therefore we observe room temperature operation.

Fig. 3.15 shows another PMOS (device D) showing strong oscillations even for very high V_D (=-0.9 V). It is an indication of a very small island with very high charging energy ($> eV_D/2$) and demonstrates operation of SET at 300 K and at supply voltages of next generation CMOS nodes.

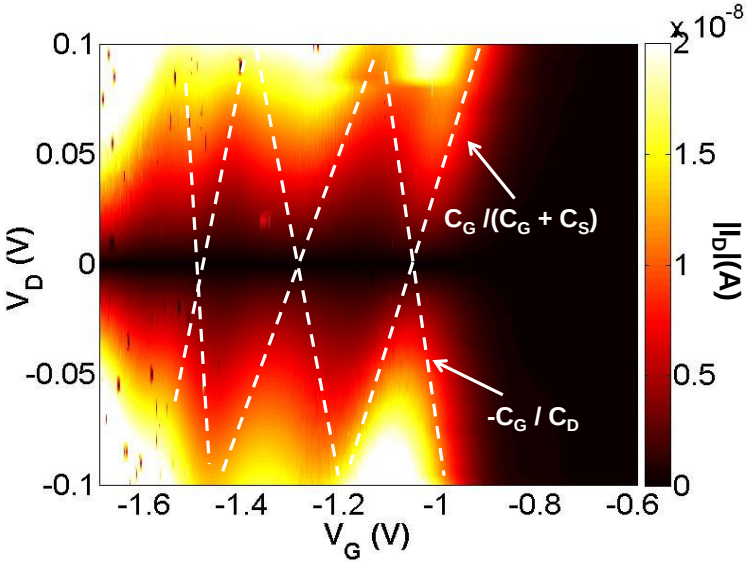


Figure 3.14: 'Coulomb Diamond' plot for the device C at 300 K. Dashed lines show the diamonds. The addition energy is estimated to be ∼85 meV.

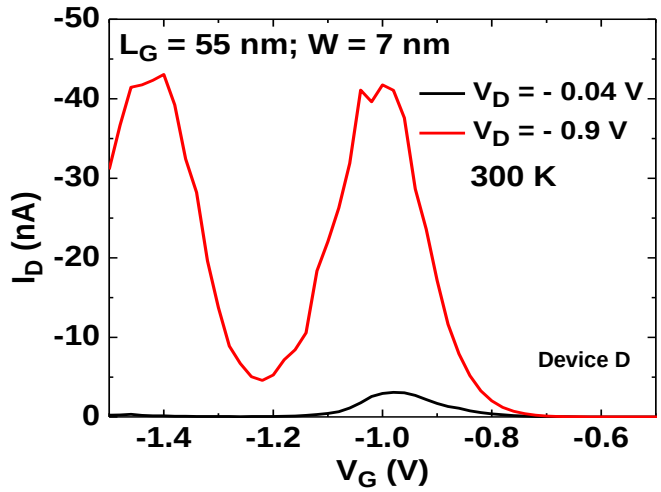


Figure 3.15: $I_D - V_G$ for a PMOS SHT with $L_G = 55$ nm showing very sharp oscillations at high V_D (= - 0.9 V) at 300 K.

3.3.2 Low Temperature Characteristics

In order to gain deeper understanding of different regimes of transport with reduced thermal excitations, low temperature measurements were performed. Differential conductance with lock-in setup (SR 830) is measured for various temperatures. Lock-in measurement helps in improving the signal to noise ratio. As we want to probe the equi-

librium properties of the system (the nanowire in our case) we measure the conductance of the device at very small AC bias (generally at about 77 Hz) such that $eV_D < \text{kT}$ (300 μV to 1 mV, for 4.2 K to 300 K). The AC voltage is applied to the drain and the source is at 'virtual DC ground' as it is connected to a 'custom' current amplifier. This amplifier converts input current to output voltage with very high gain (typically 10^8) and then feeds the signal to the lock-in. Figure 3.16 shows the schematic of the connections made to the device for measuring differential conductance with lock-in.

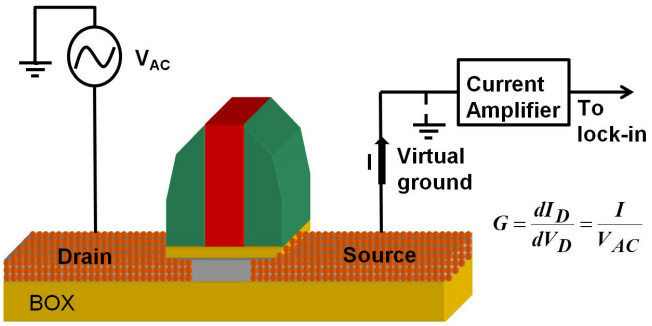


Figure 3.16: Schematic of the ac lock-in technique used in the low temperature transport measurements. Lock-in measures differential conductance, for linear regime, it will be conductance (G). Hence current I_D is $G \times V_{AC}$.

3.3.2.1 NW-MOSFET at Low Temperature

Fig. 3.17 shows the evolution of conductance, $G - V_G$ with temperature for NW-MOSFET (device E) with W=7 nm. At 4.2 K clear Coulomb oscillations are observed. For the NW-MOSFET with classical FET characteristics at 300 K, the channel potential is relatively smooth, so the barrier for confinement of electrons in the channel is not due to disorder as in the case of room temperature MOSSET (cf. previous section). These 5-7 nm wide nanowire MOSFETs have longer spacers (CD spacer = 25 nm). So the LDD extension does not reach the gate and we are in a doping 'underlap' situation. Therefore potential barriers are formed below the spacers as gate does not have control over this undoped region. As temperature is reduced, electrons can no longer surmount these barriers (barrier height ~30 meV, Thesis M. Pierre) and they play the role of 'tunnel barriers'. Thus the channel becomes an island with self-aligned tunnel barriers. In fact our group at CEA-LETI and INAC has previously demonstrated a simple and controlled method for making SET from nanowire MOSFETs exploiting this mechanism [Hofh 06]. One point to be stressed here is the mechanism of tunnel barrier

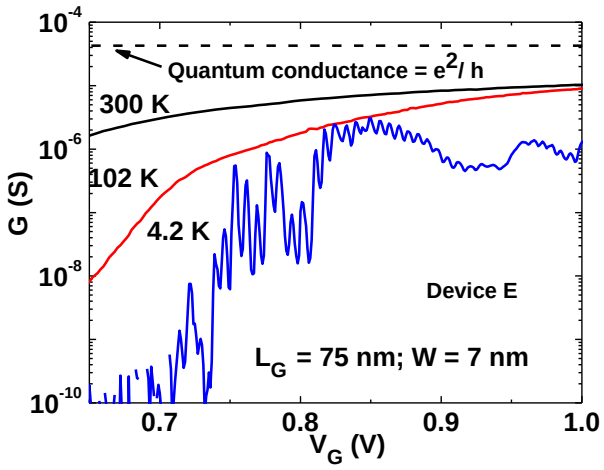
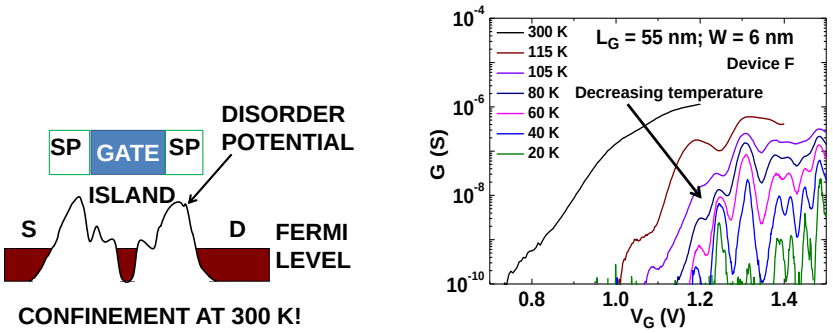


Figure 3.17: $G - V_G$ evolution with temperature for a NMOS with classical MOSFET characteristics at 300 K. Since channel potential is smooth (FET case), confinement occurs only at 4.2 K due to potential barriers below spacers

formation below the spacers. As region below spacers is undoped (or very lightly doped from diffusing dopants), it behaves as disordered insulator. These disordered insulators turn into tunnel barriers at low temperature. A detailed discussion on this can be seen in ref [Hofh 07]. The period of oscillations ($e/C_G = \Delta\ V_G \sim 6$ mV) is consistent with the geometrical gate capacitance of the device (∼28 aF for L_G=75 nm) showing that the island is defined by the whole channel.

3.3.2.2 RT-MOSSET at low temperature

Figure 3.19b shows the evolution of $G - V_G$ with temperature for a RT-MOSSET type device (device F, oscillations at 300 K similar to B, C and D) with strong Coulomb oscillations already visible at 115 K. Unlike device E, C_G for device F does not correspond to geometrical L_G, indicating smaller island in channel created by disorder and not by spacers. At lower temperatures the peaks split into multiple peaks either due to multiple islands or well-resolved addition spectrum (single-particle quantum levels shifted by charging energy). An important point is to be noted in all these observations: Oscillations (or peaks and valleys) in drain current (either at low temperature or room temperature) in ultra-scaled NWs are often interpreted as result of diffusive transport through multiple 1D sub-bands [Sing 06, Yi 11]. It is clearly seen that conductance of the NW-MOSFETs is always much below quantum conductance ($G_Q \sim 4\times10^{-5}$ S).



(a) (b)

Figure 3.18: G-V_G evolution with temperature for a NMOS showing Coulomb oscillations at 300 K. Higher V_G period due to high charging energy is observed. As shown in schematic (a), channel potential is disordered and leads to a small island and hence confinement occurs at 300 K! Note that unlike in schematic of Fig. 8a island is not due to spacers.

But, for multiple sub-band population, it should be higher than G_Q. Also, in case of ballistic transport through these sub-bands the conductance increases in steps (step height equal to quantum conductance) [Akha 10a]. Thus, our results strongly indicate that the interpretation based on multiple sub-band population may be erroneous and disorder in sub-10 nm NWs enhances island formation and results in oscillations due to single electron charging (even at 300 K).

3.4 Limitations of RT-MOSSET by Disorder and Solutions

Though scaling NW-MOSFET channel width to 5-7 nm and below enables realization of excellent RT-MOSSETs, it has its own limitations. One of the major limitation is the mechanism of island and tunnel barrier formation. As discussed in the last section we have argued that the island and tunnel barriers are formed by disorder potential of the nanowire. By its very nature, island formation in this way is stochastic. This introduces a large variability in resulting SET characteristics. Therefore, the next step is to overcome this challenge. This means we have to design a scheme where island and tunnel barriers are formed in controlled and self-aligned manner.

In section 3.3.2.1, we have discussed formation of SET at low temperature in NW-MOSFET from confinement induced by potential barriers below the spacers. This

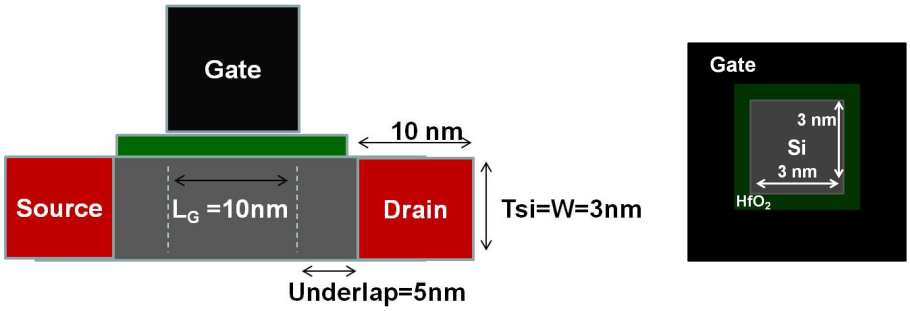
method is very robust and can lead to controlled SET characteristics [Hofh 06] as tunnel barriers are self aligned and island size is controlled (by geometrical size of the channel). On this basis, a CMOS technological platform for realizing various single electron devices (SET, Coupled double or triple dots, charge qbit devices, electron pumps etc.) was realized by our group at CEA-LETI & INAC [Paul 11] under a EU collaboration project AFSID. But it should be noted that, to date, these doping modulation SETs operate only at low temperature. So the idea of scaling the size of doping modulation SET seems encouraging for obtaining controlled RT-SET. Ultrascaled channel would increase charging energy (hence operating temperature) and doping modulation would create self-aligned, controlled tunnel barriers and island. Then we would have a well-controlled RT-MOSSET. In fact, the MOSSET presented here were fabricated with this aim. They had ultrascaled channel for increasing charging energy, with doping 'underlap' realized by using large spacers on W = 5-7 nm NWs. However, as we have noticed, for 5-7 nm width nanowires the process induced disorder dominates the transport in the device making the SET stochastic. Also, we need to pay close attention to the efficiency of undoped silicon as tunnel barriers at 300 K. It is not obvious or can not be assumed in a straightforward manner that the undoped regions below spacers would act as efficient barriers at room temperature. From the previous estimations of barrier height of around 30 meV for such barriers, it may not be sufficient to confine electrons at 300 K. We will now discuss in detail on these challenges to propose possible solutions.

3.4.1 Controlled RT-MOSSET: Are 'underlaps' the way?

Controlled room temperature MOSSET operation needs to overcome process induced disorder and have well-controlled tunnel barriers that enable island size definition. We mentioned that doping 'underlap' can produce well-controlled MOSSETs whose island size is determined by the channel dimensions of the MOSSET. However we also noticed that scaling the nanowire size (to increase operating temperature) in 'doping modulation SET' has serious challenges from disorder. Surface roughness is a major source of disorder in sub-10 nm nanowires. Therefore, in order to be free from this disorder we need to fabricate nanowires with very less line edge roughness (LER).i.e. the nanowire surface should be very smooth. As discussed before in section 3.1, hydrogen annealing after nanowire etching can 'round' the surface, smoothening it and thus

reducing the LER. This effect has been demonstrated in ref [Bang 09], wherein they have shown that LER for RIE etched NWs (down to 5 nm width) is about 1.5 nm but can be reduced to about 0.5 nm with H_2 anneal. We expect to have similar LER of about 1.5 nm, as we only have RIE etched nanowires. So we could employ H_2 anneal to improve LER of our nanowires. However, hydrogen annealing can lead to fragmentation and breaking of nanowires when width is below 15 nm. Therefore it can not be used on sub-10 nm nanowires directly. One possible way to overcome this problem would be to etch nanowires with width between 15-20 nm, reduce LER with H_2 anneal and then oxidize them to reduce the width. This oxide can be etched thereafter leaving sub-10 nm nanowires with small LER. Since the oxide layer to be etched is not so thick (about 5-10 nm) it can be optimized to minimize consumption of BOX during oxide etching, so that we can preserve the trigate (or omega gate in this case) geometry.

Now for the tunnel barriers, it is important to know if 'underlaps' can actually be efficient tunnel barriers at room temperature. So in order to verify it, we resort to 3D transport simulation in NW-MOSFETs. We use a custom made 3D NEGF (non equilibrium green's function) real-space simulator (developed at LETI, with numerical scheme similar to ref [Sviz 02] and [Poli 09]). The NEGF code employed in the simulator only includes ballistic transport with optical phonon scattering. No other scattering mechanisms are included. Also, another import thing to note is that the NEFG algorithm does not include 'electron-electron' correlations and is based on mean-field approximation [Indl 06]. This means that the Coulomb blockade effect is not accounted for in the transport characteristics. However, for the first order, we can estimate the level separation in the NW channel and also confirm confinement by undoped regions as tunnel barriers. So it can be viewed as test for 'best case scenario' for MOSSET with underlaps as tunnel barriers. If tunnel barriers are insufficient to confine electron in this case, then just underlaps would not be sufficient to realize RT-MOSSET in real case. Figure 3.19a shows the device structure used for 3D real space NEGF simulations. The $I_D - V_G$ characteristics of the device at 300 K and 77 K are at $V_D = 10$ mV are shown in figure 3.20. Oscillations are observed at 77 K due to transport through different confined levels in the channel. Since the nanowire being simulated is very small (W = 3 nm), it can have 1D levels with appreciable separation. Therefore we need to be sure that the oscillations originate from 0D island formed by longitudinal confinement and not from 1D levels of nanowire. It was confirmed that these levels belong to 0D 'island'



(a) (b)

Figure 3.19: Device structure used for 3D real space NEGF simulations. (a)Schematic of the device along the transport direction. (b) Schematic of the cross section of the device along the width. It has a square nanowire channel with edge length = 3 nm. The gate oxide is 1 nm HfO_2. It has a GAA geometry. The source/drain lengths are assumed to be 10 nm.

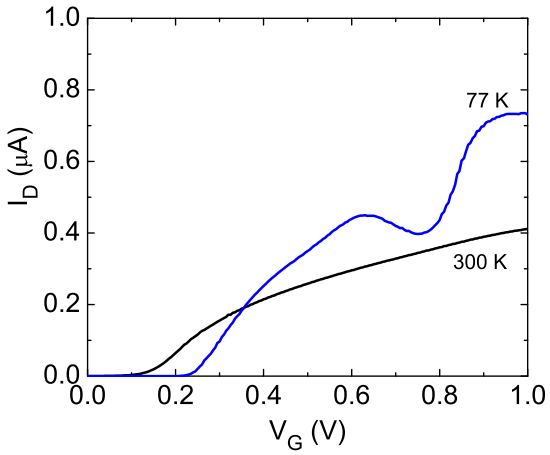


Figure 3.20: $I_D - V_G$ characteristics of the device at 300 K and 77 K at V_D = 10 mV. Oscillations are observed at 77 K due transport through confined levels in the channel island

.

formed by underlaps and not to 1D levels of the nanowire by simulating 'non-underlap' case at 77 K (curves not shown here). 'Non-underlap' case shows 'step-like' feature in the current at 77 K, matching with similar simulation results as in ref [Akha 10b]. As a further confirmation, the 2D current density plot (cross section taken in middle of NW along the length) of the device along with first sub-band edge (red line) is shown in figure 3.21. One can clearly see the tunnel barrier formation due to underlaps (red line) in the first sub-band edge. The 3D confinement of carriers leading to an island

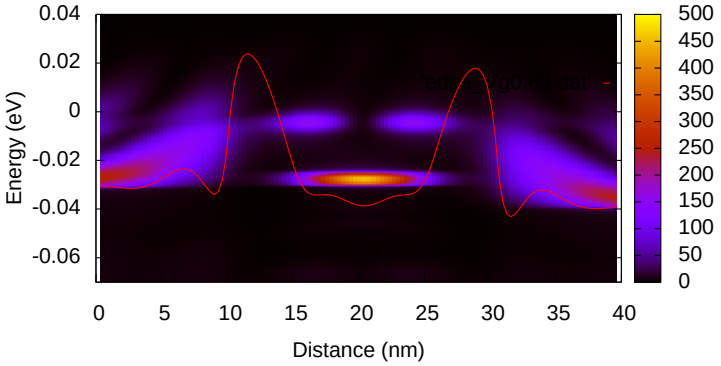


Figure 3.21: Density of states (DOS) along the the nanowire at 77 K and $V_G = 0.63$ V corresponding to the peak. Red line is the first sub-band edge, clearly showing tunnel barrier formation due to underlaps. Formation of 0D states due to 3D confinement is clearly visible in the channel. Fermi level at source (left) is set at 0 on the energy scale. DOS is in arbitrary units.

formation in channel also shows clearly separated 0D or 'quantum dot' levels. The oscillations in $I_D - V_G$ curves occur due transport through these states. We observe a peak when a level is aligned to the fermi level at source and a valley when fermi level at source is between two states in the channel. Again, we reiterate that these peaks are only due to quantum levels of the dot and not due to Coulomb blockade. Currently it is numerically very expensive to include full electron-electron correlations in the NEGF algorithm to simulate SET. But we obtain a good estimate of the quantum level separation. Coulomb blockade introduces additional energy separation over these levels, thus the dot has much higher total addition energy.

The $I_D - V_G$ curves at 300 K do not show any oscillations. This means that the barriers are not sufficient to confine the electrons in the channel to create an island. Therefore, from these simulations we can conclude that the 'underlaps' alone are not sufficient to confine electrons in the channel at 300 K. One way to go further can be to increase this barrier height. It could be done by 'counter doping' as in the case of halo doping in MOSFETs. Instead of leaving the underlaps undoped, we can dope it lightly (about 10^{16} to 10^{17} cm^{-3}) with a doping type opposite to that of source/drain. i.e. having p type LDD for a NMOS. This will increase the barrier height and may be sufficient to confine electrons at 300 K.

3.4.2 Tunnel Barrier Options: Schottky Barrier MOSSET

One can also look for other ways to realize tunnel barriers in the nanowire channel apart from doping modulation technique. However, these should be easy to integrate in the CMOS integration scheme and should not be a problem for classical FETs that need to be cointegrated alongside the MOSSETs. One such possibility is using 'Schottky' tunnel barriers. It has been proposed and demonstrated through simulation that one can realize a MOSSET using 'Schottky barrier' obtained from the silicide. As silicidation is a part of standard CMOS process flow, it can be readily used for MOSSET scheme. One work on bottom-up CVD grown Si nanowires has shown SET realized from silicide source/drain [Zwan 09]. Very small dot size was achieved by pushing the silicide junctions on either side very close to each other (about ∼6 nm separation). So it can be a possible option to realize a MOSSET. In order to verify that we measured Schottky source/drain MOSFETs fabricated on SOI at LETI. The detailed integration scheme of the devices is given in ref [Vine 09]. The devices were dopant segregated Schottky MOSFETs. Dopant segregation means piling up of dopants at the silicon-silicide interface [Kino 04]. This was done through implantation before silicide in order to reduce the very high intrinsic Schottky barrier of NiSi for NMOS (about 0.45 eV) and PtSi for PMOS(about 0.25 eV). Room temperature $I_D - V_D$ measurements were done to study ambipolar behavior and confirm the Schottky injection mechanism in the devices. The details this ambipolarity analysis are given in Appendix A.2. The device characterized were much larger than the NW-MOSFETs presented previously. Typically, the gate length ranged from 50-100 nm and the smallest width was about 350 nm. Therefore any single electron effects could only be observed at low temperature. The device transfer characteristics at low temperature are shown in figure 3.22. It can be seen that the classical FET $I_D - V_G$ develops a 'kink' or shoulder like feature at lower temperatures. It becomes prominent with decreasing temperature. At 77 K it is clearly observable. The observed features can be explained in terms of the change in relative contributions of various transport mechanisms involved in charge transport across the Schottky barrier at source side. Figure 3.23 shows the band diagram of conduction band at the source junction of the MOSFET just below the gate oxide layer.

It is well known that three mechanisms contribute to transport across Schottky barrier namely, thermionic emission over the barrier (TE), thermal-field emission (TFE)

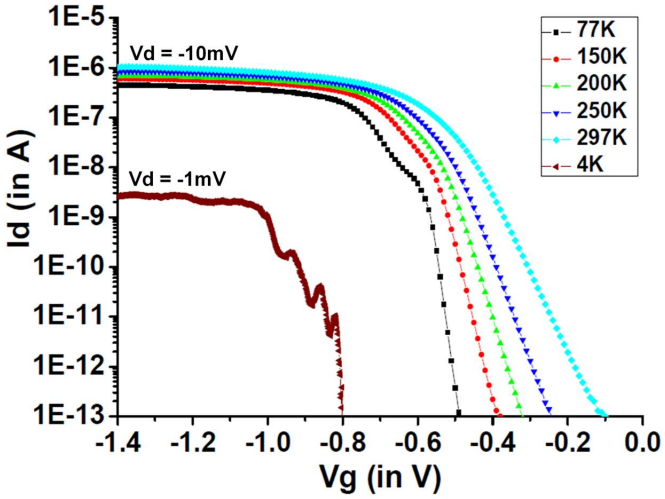


Figure 3.22: Id-Vg curves of the Schottky MOSFET from 300K to 4K. Device dimensions: L_G = 100nm, W = 500nm.

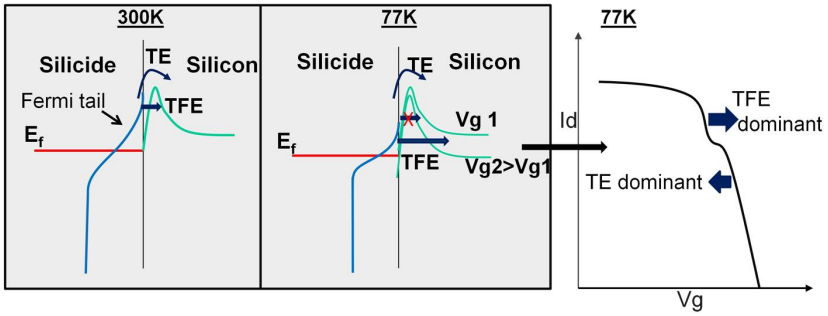


Figure 3.23: Simplified band configuration at the source Schottky barrier of the MOSFET at various Vg and temperatures. The schematic explains of the origin of 'plateau' at low temperature from difference in TE and TFE contributions.

of Fermi distributed electrons by tunneling through depletion region in semiconductor and field emission (FE) tunneling of electrons at Fermi level of the source across the depletion region. Since tunneling current decreases exponentially with barrier width, FE can occur only at high V_G and V_D values when barrier is sufficiently thin at Fermi level of source. In the subthreshold region contribution from FE is negligible and TE and TFE are major contributors. At 300K, in the subthreshold region total drain current is the sum of TE current and TFE current. Due to considerably long 'Fermi tail' (figure 3.23) both TE and TFE start contributing almost in tandem and TE itself being quite high. As temperature decreases, the 'Fermi tail' in the source shortens (figure 3.23

shows the configuration at 77K). Therefore, TE decreases along with almost complete suppression of TFE at low Vg. However, as Vg increases TE slightly saturates due to less number energetic carries 'over the barrier' at low temperature. This leads to the 'plateau' region in Id. When Vg increases further making the barrier thinner, TFE starts contributing and drain current starts increasing exponentially again. Thus, we can identify two regions in drain current with dominance of different mechanisms in the transport. It is observed that at 4.2 K, the TE part of Id is completely suppressed and transport occurs only due to tunneling. In this configuration multiple peaks are noticed in the Id-Vg curve. This can be due to single charge tunneling phenomenon with the transistor acting as a SET as proposed in previous theoretical work [Fuku 97]. So we have demonstrated a possibility of Schottky barrier MOSSET. It has to be scaled further to NW-MOSFET to study and realize room temperature operation.

3.5 Summary

This chapter focused on conception, development and characterization of room temperature (RT) operating full CMOS integrated SET. We termed the CMOS based SET as *MOSSET*. The charging energy (or addition energy) requirement of about 100 meV (or greater) for RT-SET implies an 'island' or nanowire channel with width around 5 nm (or less). End-of-roadmap (8 nm node) trigate nanowire (NW)-MOSFETs also need to have channel width of 5 nm (from scaling rules). Thus with similar nanowire channel requirements, development of a common CMOS integration scheme not only benefits both and but also integrates SET into CMOS technology, making it a *mainstream* device. The major aspects of MOSSET discussed, developed and demonstrated in this chapter can be summarized as follows:

- We developed and demonstrated a single integration scheme to realize scaled NW-MOSFETs and RT-MOSSETs on SOI. This integration scheme features high-k dielectric as gate oxide and metallic gate stack. We realized two splits in nanowire width: W (average) = 20 nm ($3\sigma = 4$ nm) and W (average) = 7 nm ($3\sigma = 3$ nm). We developed an innovative technique of 'resist trimming' to reach nanowire width down to 5 nm with optical lithography (193 nm DUV) alone.

- In the Trigate NW-MOSFETs realized in our integration scheme, we demonstrated excellent electrostatic control and scalability. Good short channel effect control was demonstrated on W =20 nm NW-MOSFETs with $DIBL = 30$ mV/V for $L_G = 20$ nm and $SS = 72$ mV/dec. For the same $L_G(= 20\ nm)$ on reducing width to 5-7 nm, $DIBL$ and SS are further reduced to 12 mV/V and 62 mV/dec respectively showing excellent SCE control with W reduction.

- In 5-7 nm width nanowires we demonstrated a transition from FET to SET characteristics(Fig. 3.12). With nominally identical device dimensions (L_G and W), one device behaves as FET and other as SET (with Coulomb oscillations) at 300 K.

- We proposed that this transition or RT-SET behavior in 5-7 nm nanowires is due to disorder potential in nanowires (for instance by surface roughness) leading to island and tunnel barrier formation. Charging of these islands leads to SET behavior. As our nanowire fabrication process is not fully optimized, we expect to have Line Edge Roughness (LER) of about 1.5 nm. On a 5 nm nanowire, such a LER can produce constrictions of about 2 nm width creating an island in between.

- Benefiting from the disorder induced island formation, we demonstrated excellent MOSSETs with sharp Coulomb oscillations at 300 K(Fig. 3.13). The addition energy$\sim$85 meV was estimated from Coulomb diamonds(Fig. 3.14).

- A device with very high addition energy (>450 meV) was shown to operate at $V_D = \pm 0.9\ V$. This demonstrates MOSSET operation at same voltage levels as next generation MOSFETs and thus paves way for seamless cointegration of SET and FET.

- Low temperature measurements on both NW-MOSFETs and RT-MOSSETs were presented. These measurements further confirm disorder induced island formation and also show Coulomb blockade in NW-MOSFETs (at 4.2 K) due to doping 'underlap'

- Disorder based MOSSETs are stochastic. So to realize a controlled MOSSET at room temperature, nanowires with smaller LER (about 0.5 nm) and controllable

tunnel barriers have to be fabricated. Smaller LER can be achieved by hydrogen annealing of 15 nm width nanowire and subsequent oxidation and etching to reduce width down to 5 nm. For controlled tunnel barriers, either 'counter doped' LDD extensions or silicide Schottky source and drain junctions can be possible options.

4

SET-FET Cointegration and Hybrid Circuits

In the previous chapter we have demonstrated a fully functional 300 K operating MOSSET with high-k/metal gate. Going a step further, in this chapter we demonstrate cointegrated SET-FET circuits showing various functionalities. We first discuss the limitations of 'pure SET based logic/memory' circuits and also highlight why it would be beneficial to rather have circuits combining the SET and the FET. We then mention some of the proposals and demonstrations of SET-FET circuits in the literature. Thereafter, we show experimentally studied SET-FET circuits at 300 K, cointegrated on the same chip. These circuits include a SET-FET based current amplifier that extends Coulomb oscillations up to milliampere range, a high PVCR ($> 10^4$) negative differential resistance circuit and a SET-FET circuit for converting the drain voltage oscillations of a current biased SET into the binary state voltage levels (0 and 1 V) of current CMOS technology.

4.1 Limitations of SET based Logic

In this section we will discuss the intrinsic limitations of the SET that lead to major challenges in a pure SET based logic scheme. Historically, the SET was mostly sought for memory operations. One of the main motives was the possibility to store one bit as a single electron. This would enable extremely high integration density of about 10^{12} bits/cm^2. Many research groups have demonstrated various memory architectures

that exploit single electron effects, either directly employing a SET (or a single electron box [Likh 99, Durr 99]) or using the island as 'single charge storage' node. One of the earliest demonstrations of such a 'single electron memory' was an ultrascaled floating gate MOSFET, where the floating gate was a nanoscale polysilicon island. Single electron charging of this island produced discrete threshold voltage shifts in the nanowire channel MOSFET [Guo 97]. However, the memory window (threshold voltage shift) and the retention of single electron in the 'floating gate island' were not sufficient enough for practical non volatile memory (NVM) applications. But this inspired a new class of NVM architecture where the continuous floating gate was replaced by many nanoscale islands (rather nanocrystals) that act as charge storage nodes to realize few electron memory [Tiwa 96, De S 03]. These were very successful, with nanocrystal charge trap memories already in advanced development stage in industries [Mura 04].

The SET based logic, however, had many intrinsic technological challenges that have hindered its progress. For realizing logic operations through SET many schemes were proposed. They could be classified as 'charge based logic' and 'voltage based logic'. Charge based logic circuits [Ono 05] utilize single electron charge as a single single bit for digital operation. The logic states 0 or 1 are defined in terms of presence or absence of a single electron charge at a particular 'node' in the circuit network. Major problem of such a logic scheme is the scalability. As the scheme works on transfer of charges among different nodes like a shift register, simple wire interconnects can not be used to extend the circuit. Each node has to be connected to adjacent nodes through a tunnel barrier such that electrons move from one node to another by tunneling. On the other hand, voltage based logic scheme basically aims to mimic the ubiquitous digital logic scheme based on the MOSFET (Transistor-Transistor-Logic: TTL). In this scheme, the SET replaces the FET to realize same logic operations as in conventional digital logic. It utilizes the SET as a switch with ON and OFF states being the 'conducting state' and 'Coulomb blockade' state respectively. The major challenge for such a scheme is the 'very high output impedance' of the SET and 'low voltage gain' of SET based circuits. This results in a small fan-out (about 1 [Zhir 05]) and low speed of the SET based logic circuits (for instance, charging time of a 100 μm long interconnect through a 100 kΩ impedance is about 1 ns [Likh 99]).

It is, therefore, more interesting to complement the CMOS logic through unique Coulomb blockade feature of the SET by combining the two. The MOSFET has a

very high current drive and high gain whereas the SET has non-monotonic, oscillatory $I_D - V_G$ characteristics. By combining these two devices into hybrid SET-FET circuits, various novel functionalities can be obtained that are absent in pure CMOS logic portfolio. Besides this, some of these SET-FET circuits can also improve existing CMOS logic circuits by reducing transistor count [Inok 03], as we will see later in this chapter. Therefore, the practical domain of the SET applications lies in hybrid SET-FET analog circuits. In this chapter, we will briefly look at various efforts already done in realizing hybrid SET-FET circuits. We will not make a comprehensive review but highlight some of the major efforts. Then we will demonstrate various hybrid SET-FET circuits at 300 K, cointegrated on the same die through our integration scheme described in the previous chapter. The ability to realize these circuits is one of the major strengths of our integration scheme that provides seamless cointegration of the MOSSET and the MOSFET. We will be focussing on a hybrid SET-FET circuit that provides SET current amplification, as proposed by SET-FET co-design work done at EPFL [Maha 05b, Ione 04]. Based on this circuit we demonstrate negative differential resistance (NDR) circuit. This NDR circuit forms the basis of 'mulitvalued memory' scheme. We also show a literal gate, which is among the basic building blocks of the 'multivalued logic' scheme.

4.2 Various Hybrid SET-FET Circuits

With the development of fabrication process for room temperature operating Si SETs, many groups have also made efforts for demonstrating different hybrid SET-FET circuits. As mentioned before, inherent drawbacks of pure SET based logic and CMOS compatible process for Si SETs were the main motivations for considerable progress made in realizing SET-FET circuits. We will briefly discuss some of these efforts.

4.2.1 SET-FET Multi Valued Logic (MVL)

Multivalued logic (MVL) is a non-binary logic where the logic transitions involve more than two states. Owing to higher number of logic states, MVL has the potential for higher data storage in less area as compared to binary logic [Maha 05b]. MVL also has potential advantage over binary that it can reduce components per logic function and also improve operating speed. Since a conventional MOSFET is a single threshold

device, obtaining multiple output states for MVL from it is not convenient. Whereas a SET, with its oscillatory $I_D - V_G$ characteristics, has multiple thresholds. Therefore it would be more suitable to realize multiple output states required for multivalued operations.

Multivalued logic functions can be constructed from the literal function (or a literal gate). Literal function is represented by a literal gate as follows: the output is 'high' if the input is within a 'specified region', otherwise it is 'low'. Suppose we have two thresholds that define the region (say a, b) and if x is the variable input, then we have the literal function as [Waho 98]:

$$output = \begin{cases} High & \text{if } a \leq x \leq b, \\ Low & \text{otherwise} \end{cases} \tag{4.1}$$

This can be extended further using the 'universal literal gate' formed by composing together many literal functions i.e.composing together many 'specified regions'. If A is the set of all specified regions we have for the literal gate [Hany 97]:

$$output = \begin{cases} High & \text{if x} \subset A, \\ Low & \text{otherwise} \end{cases} \tag{4.2}$$

Thus these gates form the basic components of MVL as they convert multivalued input levels into a sequence of binary output levels.

Connecting a SET and a FET in series, Inokawa et al. [Inok 01a, Inok 03] have proposed a SET-FET circuit that functions as a 'universal literal gate'. In order to achieve universal literal gate output, this circuit converts the voltage oscillations of a current biased SET (which are usually in millivolt range) into voltage levels compatible with binary states of conventional CMOS circuits (typically 1-5 V). Figure 4.1 shows the circuit diagram of the SET-FET universal literal gate. Here, the FET is connected to the SET in series and the FET is biased by a constant current (CC) load I_o. The output is taken at the drain terminal of the FET. The FET gate is kept at constant voltage V_{gg} such that there is a fixed voltage, $V_{gg} - V_{th}$ (V_{th}-threshold voltage of the FET), at the drain of the SET. This voltage ($V_{gg} - V_{th}$) is so adjusted as to sustain Coulomb oscillations in the SET. With the CC load connected, when gate voltage of the SET (V_{in}) is swept from low to high, the output voltage (V_{out}) oscillates as per the Coulomb oscillations in the drain voltage of the SET. Therefore current I_o is so chosen as to get maximum voltage swing at output for the oscillations. Figure 4.1b shows the

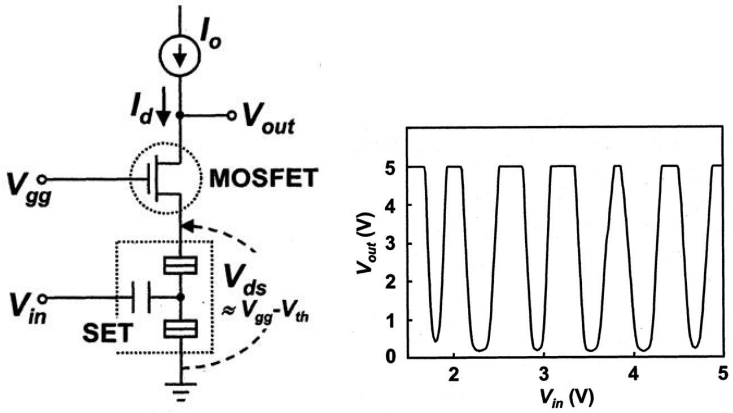


Figure 4.1: (a) Circuit schematic of the universal literal gate. It consists of a SET and a MOSFET connected in series. The MOSFET is biased by a constant current (CC) load. (b) Measured $V_{out} - V_{in}$ characteristics of the universal literal gate at 27 K. Compliance voltage at the output is set at 5 V. Figure from [Inok 03].

measured characteristics of the literal gate at 27 K. Lower temperature operation of the circuit is attributed to the SET operation temperature. With this universal literal gate they have also demonstrated MVL circuit applications like a quantizer for digital communication systems. The measurement setup of the quantizer and the measured characteristics are shown in figure 4.2. This quantizer circuit is further used in a 3-bit ADC in ref [Inok 03]. Such a SET-FET ADC has lesser components (n, for n-bit) as compared to pure FET based flash ADC ($n^2 - 1$, for n-bit).

Recently research group from Samsung and Chungbuk National Univ., Korea have also demonstrated a SET-FET circuit for multivalued exclusive-OR (MV-XOR) logic gate [Kim 09]. The circuit schematic of the SET-FET MV-XOR logic gate and truth table for the circuit is shown in figure 4.3a. Figure 4.3b shows the measured $V_{out} - V_{in}$ characteristics as a 2D color plot for the MV-XOR logic gate at 7 K. Here as well, the SET operates only at low temperatures.

4.2.2 SET-FET Amplifier and Inverter

It is well known that the major limitation of the SET is its high output impedance and low drive current. We have mentioned earlier that this could be alleviated by amplifying the current of the SET with a MOSFET. Researchers from EPFL have

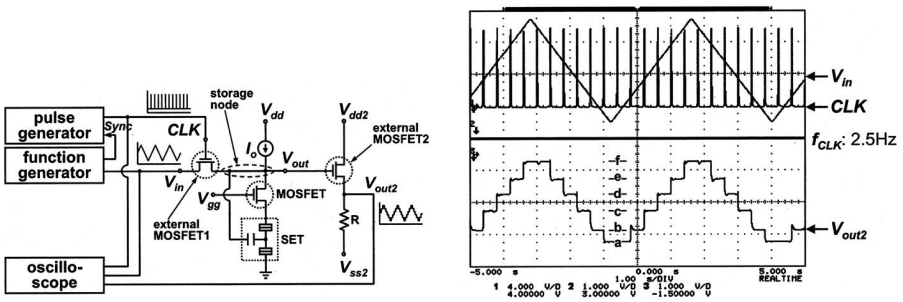


Figure 4.2: (a) Measurement setup for the quantizer crcuit [Inok 03]. (b) Quantizer operation measured by the setup in (a), with V_{gg} of 1.08 V and a CC load of 4.5 nA. Operation speed is not limited by the intrinsic performance of the device but by the large stray capacitance of 370 pF at V_{out}

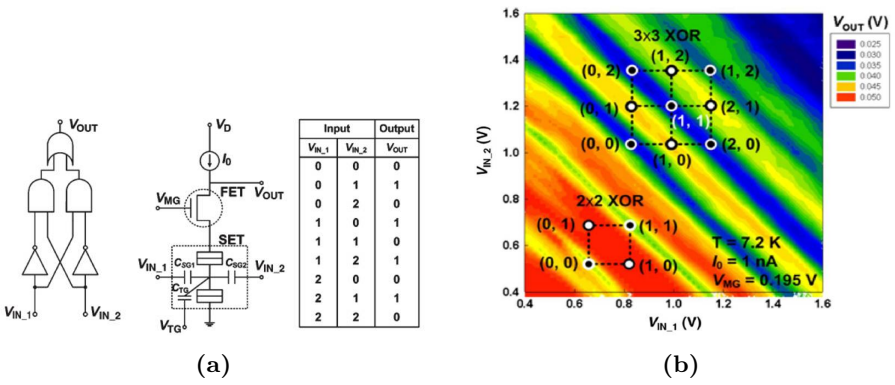


Figure 4.3: (a)(Left to right) Logic diagram of the CMOS XOR requiring at least 16 transistors. Circuit schematic of the SET-FET multivalued XOR logic gate. Truth table of for the MV-XOR logic gate (b) 2D color plot of $V_{out} - V_{in}$ characteristics of the MV-XOR logic gate at 7 K. Figures from ref [Kim 09].

proposed a SET-FET circuit wherein a FET acts as current amplifier for the SET and the output is amplified oscillating current. Figure 4.4 shows the schematic of such an amplifier circuit and its characteristics as proposed in a simulation work by Mahapatra et al. [Maha 03, Ione 04]. The circuit was named as 'SETMOS' circuit. Here, the SET is current biased and the MOSFET gate terminal is shorted to the drain of the SET. The MOSFET is kept in voltage bias mode. The drain voltage of a current biased SET oscillates when its gate voltage is swept. Now this oscillating voltage is applied to the gate of the MOSFET. Therefore the drain current of the MOSFET (with its

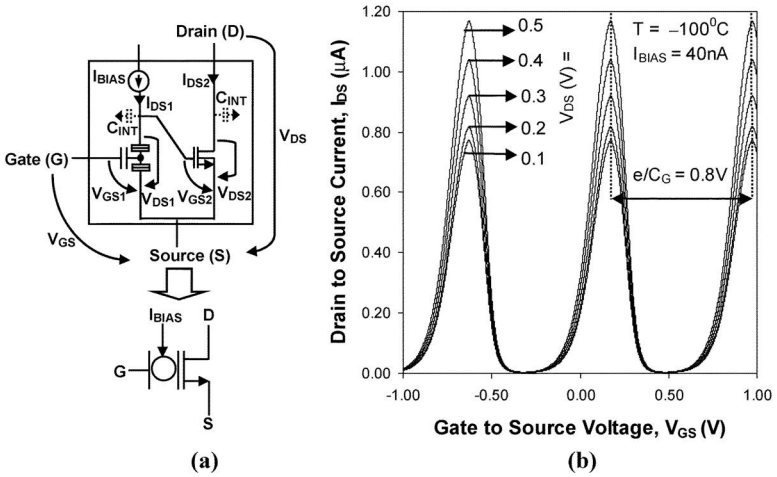


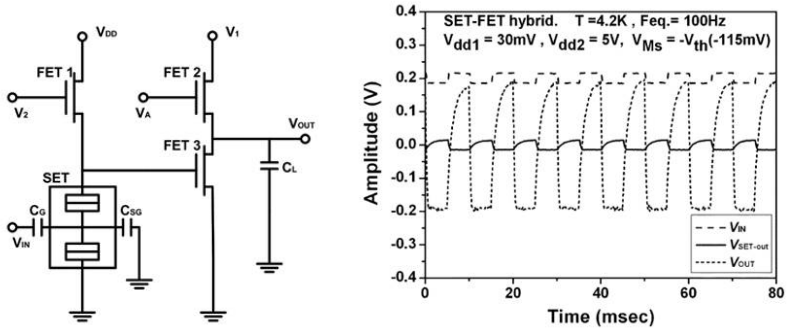
Figure 4.4: (a) Circuit schematic of SETMOS [Ione 04]. (b) Simulated $I_D - V_G$ characteristics of SETMOS, showing SET current amplification to microampere range.

drain voltage held constant) also oscillates, leading to current amplification. Thus the Coulomb oscillations of the SET are extended in the drain current of the MOSFET (in microamapere range) To get the best amplification, the MOSFET has to be operated in sub-threshold ('weak inversion') region as its drain current is very sensitive to changes of few mV on the gate in this region. The SET drain voltage oscillation peak has to be closer to V_T of the MOSFET. The output of the SETMOS (drain current of the MOSFET) is given by:

$$I_{DS} \propto exp(\frac{V_{GS2}}{\eta V_T}) = exp(\frac{V_{DS1}}{\eta V_T}) \tag{4.3}$$

where, V_{GS2} is the voltage on the MOSFET gate and is equal to the drain voltage of the SET, V_{DS1}; η is the subthreshold slope factor. This circuit will be discussed in detail in the next section along with experimental realization.

Another circuit similar to SETMOS was experimentally demonstrated by Park et al [Park 05]. Here the SETMOS circuit was extended to obtain an output voltage driver circuit. The circuit schematic and measured characteristics are shown in figure 4.5. Here, the SET is current biased by a MOSFET (FET_1, figure 4.5a) acting as a current source. The MOSFET is also current biased (by another MOSFET as current source) and the output voltage is the voltage at the MOSFET drain terminal. The circuit amplifies the voltage applied at the input (gate voltage of the SET) by one order of magnitude. The input voltage is provided at the drain terminal of this MOSFET. As the SET operates at low temperature, the measurements are done at 4.2 K.



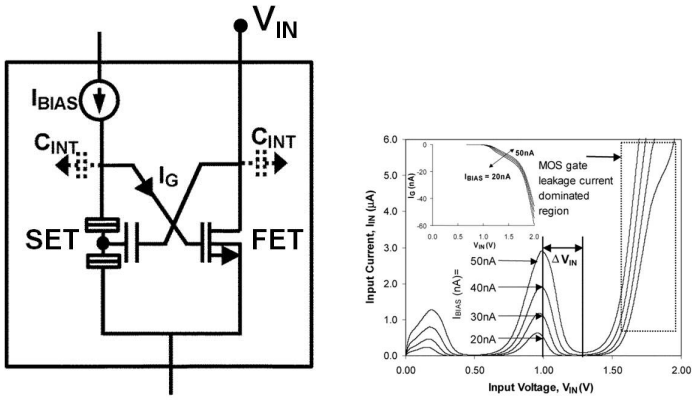
(a) **(b)**

Figure 4.5: (a) SET-FET output driver circuit schematic. [Park 05] (b) Output driver circuit showing inverting and amplifying characteristics.

4.2.3 Negative Differential Resistance (NDR) circuit

The SET owing to its Coulomb blockade characteristics has negative transconductance ($\frac{dI_D}{dV_G} < 0$) region in its $I_D - V_G$ characteristics. This enables one to build complimentary circuits from just one type of SET, unlike the case of a FET where we need n-type and p-type FETs. However, its functionality could be greatly extended if it one could obtain negative 'output conductance($\frac{dI_D}{dV_D}$)' or negative differential resistance from it. Quite early on, such a NDR circuit comprising of a SET and a single electron box (connected to each other) was proposed by Heij et al [Heij 99]. However, this was a fully SET based circuit. On similar lines, extending their previous work on SETMOS, Mahapatra et al. also proposed and demonstrated, through simulations, a NDR circuit comprising of a SET and a FET [Ione 04]. This circuit has similar connections as in the SETMOS (with the SET being current biased), but additionally in this circuit, the drain of the MOSFET is shorted with the gate terminal of the SET. The schematic of the NDR circuit and the simulated $I - V$ characteristics are shown in figure 4.6. Here only the drain voltage of the MOSFET is varied and the drain current is recorded. A feedback loop is created by the SET and the current bias source (I_{BIAS}) which leads to decrease in the drain current of the MOSFET when the SET is in positive transconductance region ($\frac{dI_D}{dV_G} > 0$). Whereas, when the SET enters negative transconductance region ($\frac{dI_D}{dV_G} < 0$) this feedback loop leads to an increase in the MOSFET drain current, thus creating a NDR region. The number of NDR peaks depends on the number of Coulomb peaks in the SET $I_D - V_G$ characteristics. Again, to get sharper NDR

peaks the MOSFET has to operated close to V_T in the weak inversion region. This circuit will also be discussed in more detail in the next section along with experimental characteristics based on our 300 K MOSSET.



(a) (b)

Figure 4.6: (a) Schematic of SETMOS based NDR circuit. (b) $I-V$ characteristics of the NDR circuit. Figures from ref [Ione 04].

The research group from NTT, who had proposed and demonstrated universal literal gate, have also extended their literal gate scheme to obtain multipeak NDR characteristics [Inok 01a]. The schematic of the NDR circuit and measured $I-V$ characteristics are shown in figure 4.7. The circuit operates at 27 K.

By current biasing the NDR circuits one can obtain hysteresis in $V-I$ curves [Inok 01a, Maha 05a]. This hysteresis characteristics is the basis of multivalued SRAM cell [Maha 05a]. Therefore, SET-FET based NDR circuit is a basic building block of the multivalued memory operation.

4.3 SET-FET Cointegration and Hybrid Circuits at 300 K

We have mentioned in the last chapter that one of the prime motivation of our MOSSET integration scheme was to develop a platform for seamless cointegration of the SET and the MOSFET. We have successfully demonstrated both the end-of-the-roadmap MOSFET and room temperature operating MOSSET through the same integration scheme. The critical process step that enables this cointegration is the nanowire patterning process. We can simultaneously pattern planar (wide area) MOSFETs, single isolated nanowires (for MOSSET) and multichannel (NW array) NW-MOSFETs. As the rest

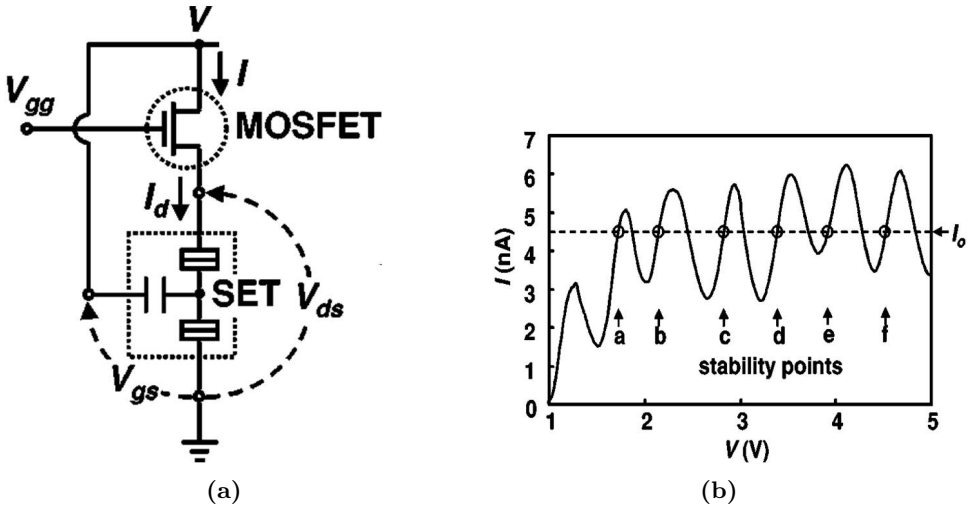


Figure 4.7: (a) Schematic of multipeak NDR circuit with a SET and a FET connected in series. A constant current source is also shown which will be used for MV memory operation. (b) $I - V$ characteristics showing multiple NDR peaks at 27 K for $V_{gg} = 1.08$ V. Figures from ref [Inok 01a].

of the integration scheme like gate patterning, source/drain formation is common for all devices, we can realize from wide planar fully depleted-SOI (FDSOI) MOSFETs to ultrascaled NW-MOSFETs along with MOSSETs on the same die. The circuit realization can then proceed through appropriate connections in the metallic layers in BEOL integration[1]. Therefore, our SET-FET circuits can be fabricated in the same way as current generation VLSI circuits. Thus, our MOSSET process technology can be easily upscaled for large area, complex circuits and can even be integrated in current VLSI design tools/platforms. In the following sections we demonstrate cointegrated SET-FET circuits showing current amplification, NDR and literal gate characteristics at 300 K. All the circuits experimentally demonstrated are similar to those proposed in simulation work of Mahapatra [Maha 05b]. To realize our circuits we use two MOSSET-MOSFET pairs , each pair from the same die on a 300 mm SOI wafer. The MOSSETs were chosen on the basis of their charging energy. This will directly translate into the effect of MOSSET scaling on these circuit characteristics. Thus, besides demonstrating the prototype circuits we also shed light on the scaling behavior.

[1]Fabrication of wafers presented in this thesis was stopped at first metal (M1) level. So the SET and FET were not connected on chip. Measurements were carried out by externally connecting them on probe station. See appendix A.3 for details.

4.3.1 SET-FET Amplifier: Oscillating FET at 300 K

In all the SET-FET circuits that we will be demonstrating here, the SET will be in current bias mode. The biasing mode of the FET will depend on the circuit under consideration. The current source for biasing the SET can, in principle, be a MOSFET current mirror or a MOSFET biased at a constant gate and drain voltage. Here we have used semiconductor parameter analyzer in current source mode. We will first look at the SET output characteristics under constant current biasing.

Figure 4.8 shows the $I_D - V_G$ characteristics of a SET (SET-A), measured at 300 K for two drain voltages V_D = 40 mV and 0.9 V. SET-A shows remarkably high V_D operation (= 0.9 V) with high peak-to-valley-current-ratio (PVCR) equal to 11. As mentioned before we have chosen the two SETs based on their charging energies. SET-A has a very high charging energy, $E_C \simeq eV_D/2$, and hence can sustain Coulomb oscillation even at a very high V_D value of 0.9 V. As seen in figure 4.8 the I_D at 'Coulomb peak' is about 1 nA for V_D = 0.9 V. Therefore, for current biasing we should choose a constant current value less than 1 nA.

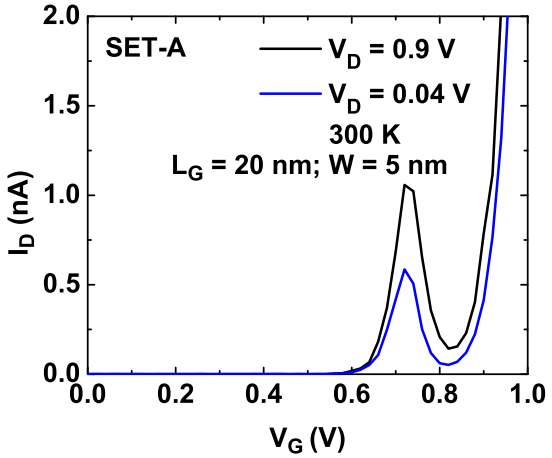


Figure 4.8: $I_D - V_G$ curves at V_D = 40 mV and 0.9 V of SET-A at 300 K showing Coulomb peak. The SET has a gate length, L_G = 20 nm and W = 5 nm. Due to very high charging energy the Coulomb peak is visible even at V_D = 0.9 V!

We denote the SET source to drain voltage drop in current bias mode as SET-V_D . The biasing current is denoted as I_{BIAS}. Figure 4.9 shows the SET-V_D -V_G characteristics at various I_{BIAS} for SET-A in current bias mode. Figure 4.9a explains the observed characteristics. We have set a compliance on SET-V_D at 1.1 V. SET-A

voltage drop has a range of one order from 1.1 V (compliance voltage) to 30 mV. This is due to high charging energy of SET-A and hence it can support high voltage drop.

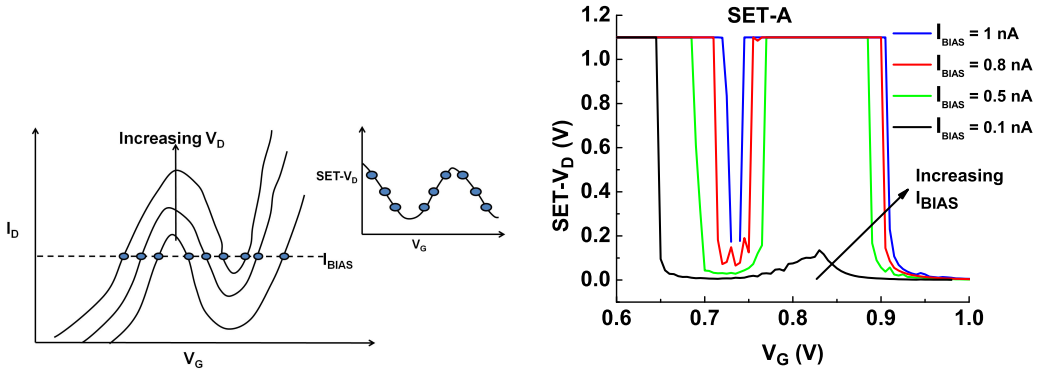
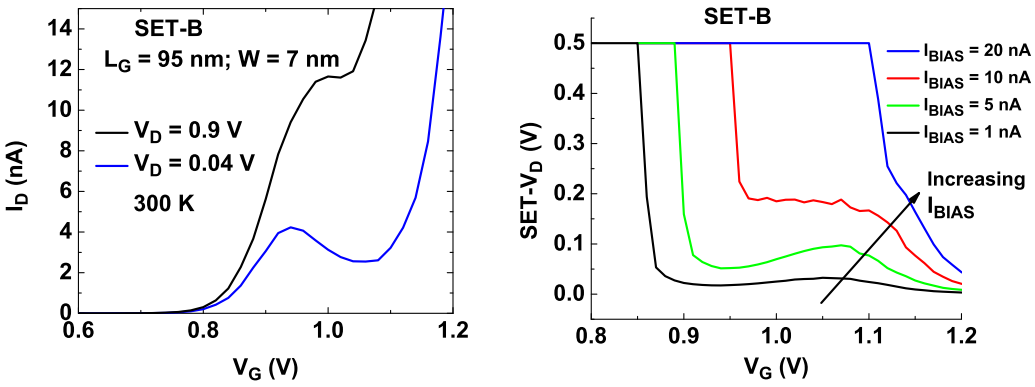


Figure 4.9: (a) Schematic explaining the $SET\text{-}V_D - V_G$ characteristics. In the $I_D - V_G$ curve constant current line is shown. When current biased, $SET\text{-}V_D$ follows this line when V_G is changed giving oscillatory $SET\text{-}V_D - V_G$ curve (inset) (b) Measured $SET\text{-}V_D - V_G$ characteristics for SET-A at 300 K. I_{BIAS} is changed from 0.1 nA to 1 nA. The oscillation broadens with increasing I_{BIAS} . Compliance for $SET\text{-}V_D$ is set at 1.1 V.

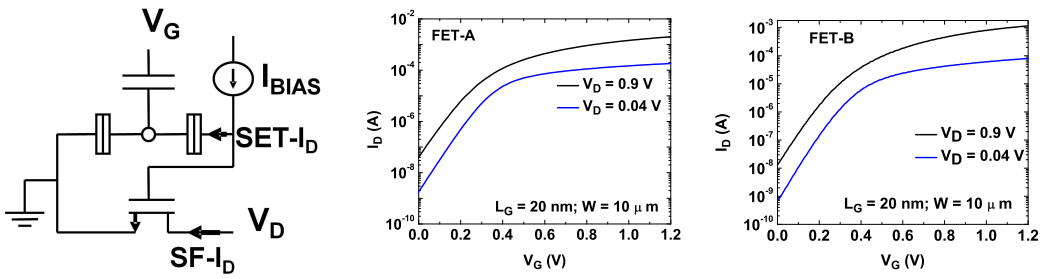
Figure 4.10a shows the $I_D - V_G$ characteristics of SET-B, measured at 300 K for two drain voltages $V_D = 40$ mV and 0.9 V. The Coulomb peak in SET-B flattens out at $V_D = 0.9$ V. So the device has no Coulomb blockade at this voltage. Therefore, it has a lower charging energy compared to SET-A and hence operates only at low V_D values. Also, the PVCR of SET-B is lower than SET-A even at $V_D = 0.04$ V. This indicates that E_C of SET-B is much lower than that of SET-A. The source-drain voltage drop $SET\text{-}V_D$ for SET-B in current bias mode is shown in figure 4.10b. As evident, SET-B V_D operation range is limited to 0.1 V. At V_D higher than that, the oscillation vanishes. Also, owing to low PVCR, $SET\text{-}V_D$ of SET-B changes by a smaller magnitude as compared to SET-A.

Now the SET-FET hybrid circuit for current amplification and the corresponding bias schemes are shown in figure 4.11a. It is same as the SETMOS circuit mentioned in the previous section (we will call it 'SF' circuit here). This circuit converts the drain voltage oscillations of a current biased SET into oscillations in the drain current of the MOSFET. Thus the output of the circuit gives Coulomb oscillations at the level of MOSFET drain current in weak inversion. As the SET is current biased, the



(a) (b)

Figure 4.10: (a) Coulomb peak of SET B. The SET has a gate length, L_G = 95 nm and W = 7 nm. SET B does not show oscillation at V_D = 0.9 V due to smaller charging energy. (b) $SET\text{-}V_D - V_G$ curves of SET-B for various I_{BIAS} . Due to low charging energy oscillation in $SET\text{-}V_D - V_G$ curve for SET-B vanishes when high I_{BIAS} (= 20 nA) is applied. Compliance is set at 0.5 V.



(a) (b) (c)

Figure 4.11: (a) Schematic of the SET-FET circuit (SF circuit) for current amplification. (b) $I_D - V_G$ at V_D = 40 mV and 0.9 V of a FET (FET-A) coupled to the SET-A in the SET-FET circuit. FET-A has a gate length L_G = 20 nm and W = 10 μm. (c)$I_D - V_G$ at V_D = 40 mV and 0.9 V of FET-B coupled to SET-B. Dimensions of FET-B are L_G = 20 nm and W = 10 μm.

drain voltage of the SET ($SET\text{-}V_D$) oscillates when gate voltage is swept from 0 to 1 V (Fig. 4.9b). Since the drain of the SET is connected to gate of the MOSFET (Fig. 4.11a), the gate voltage of the MOSFET follows $SET\text{-}V_D$. Therefore the gate voltage of the MOSFET oscillates producing oscillations in the drain current for the corresponding region of the MOSFET $I_D - V_G$ curve. This is explained qualitatively by the schematic in figure 4.12.

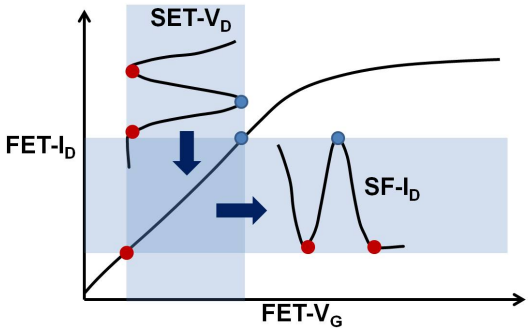


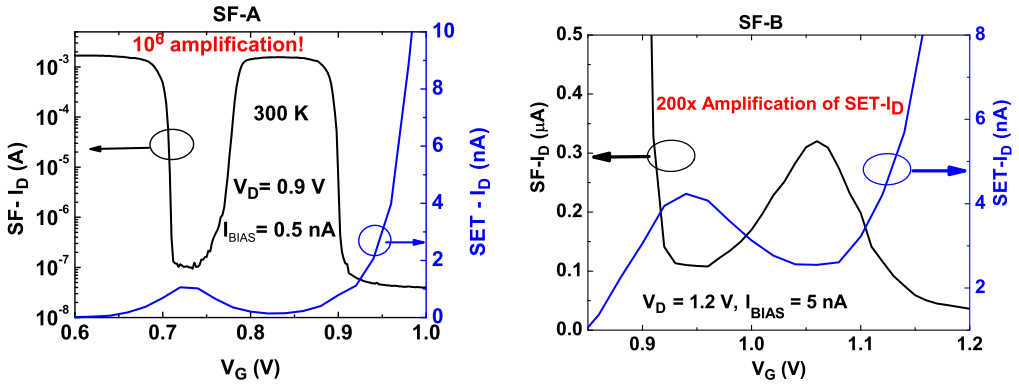
Figure 4.12: Schematic explaining qualitatively the output of the current amplifier SET-FET hybrid circuit (SF circuit).

From the figure 4.12 it is clear that in order to get best amplification from the circuit, the peak of $SET - V_D$ oscillations (marked by blue dot) has to be closer to the threshold voltage (V_T) of the MOSFET. This ensures larger amplification as the MOSFET drain current is very sensitive to small changes in its gate voltage in the subthreshold region. Therefore the output of the circuit ($SF - I_D$) can be given by:

$$SF - I_D \propto exp(\frac{FET - V_G}{\eta V_T}) = exp(\frac{SET - V_D}{\eta V_T}) \tag{4.4}$$

This equation only describes the SF output when $SET - V_D$ range is limited to sub-threshold part of the MOSFET $I_D - V_G$ curve. However, as we will see later in this section, the $SET - V_D$ for SET-A covers the region above threshold of the MOSFET. In that region $SF - I_D$ is directly proportional to $FET - I_D$ above threshold. So $SF - I_D$ can also saturate if $FET - I_D$ saturates.

Figures 4.11b and 4.11c show the FETs (FET-A and FET-B resp.) connected to the SETs (SET-A and SET-B) in the SF circuits. Both the FETs have similar dimensions and similar $I_D - V_G$ characteristics. Hence the resulting SF characteristics will depend directly on the SETs. The circuit comprising of SET-A and FET-A is named SF-A and that formed from SET-B and FET-B is named SF-B. SF-A $I_D - V_G$ is shown in figure 4.13a. It can be seen that SF-A achieves 10^6 amplification of SET-A I_D, which is also shown alongside for comparison. As SET-V_D of SET-A (Fig. 4.9b) covers entire V_G range of FET-A, output of SF-A becomes equivalent to an oscillating FET, with SF-A output going from few nA in OFF state to a mA in ON state and back. Note that the level of current in the ON state is same as that of FET-A (Fig. 4.11b). SF-B $I_D - V_G$ is shown in figure 4.13b. SF-B only shows an amplification of 200. As



(a) $I_D - V_G$ of SF-A with $I_{BIAS} = 0.5$ nA on SET-A, $V_D = 0.9$ V on the MOSFET at 300 K. SET-A current is amplified by 10^6 times leading to miliampere range oscillations. Also the dynamic range of oscillations is very high, more than 4 orders of magnitude between peak and valley current.

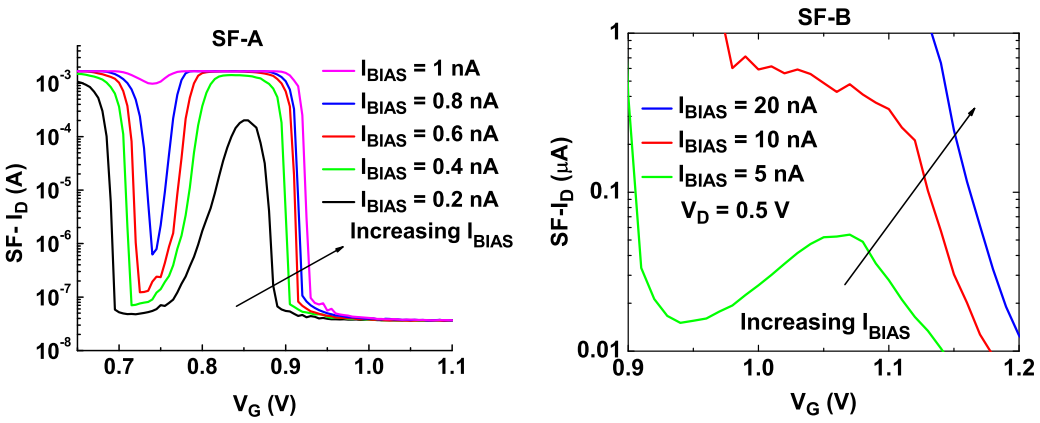
(b) $I_D - V_G$ of SF-B with $I_{BIAS} = 5$ nA on SET-B, $V_D = 1.2$ V on the MOSFET at 300 K. $I_D - V_G$ of SET-B at $V_D = 40$ mV is also shown alongside for comparison. SET-B output current is amplified 200 times in SF output.

Figure 4.13: SF circuit characteristics.

SET-V_D of SET-B only reaches a maximum of 0.1 V (Fig. 4.10b), the FET-B operates in subthreshold regime (Fig. 4.11c), where drain current is small. Hence the lower amplification. Also, the PVCR of SF-B oscillations is small, which is due to small PVCR of SET-B. In figure 4.14 we show the effect of SET bias current (I_{BIAS}) on SF circuits. Increasing bias current increases the voltage drop (SET-V_D) across the SET, broadening and eventually flattening out the Coulomb peak. Hence SF-I_D broadens and sharpness of oscillations decreases with increasing I_{BIAS} .

4.3.2 Negative Differential Resistance (NDR) Circuit

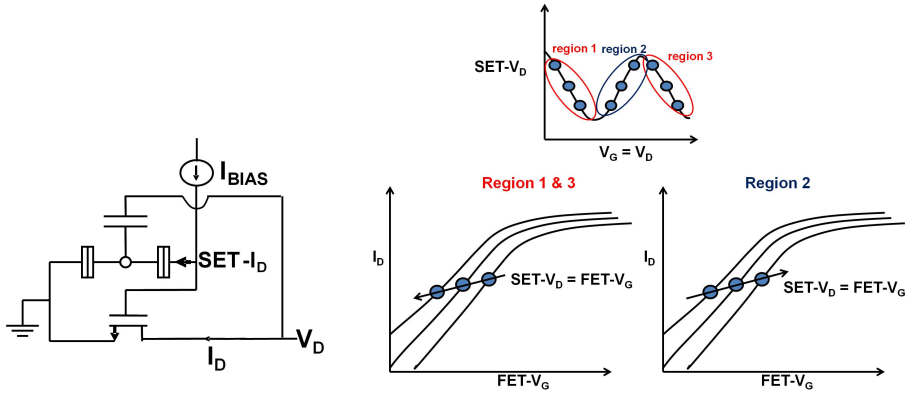
The negative differential resistance (NDR) characteristics can be obtained from the SF circuit by shorting the drain of the MOSFET with the gate of the SET. The circuit schematic is shown in figure 4.15a. Figure 4.15b qualitatively explains how the NDR characteristics are produced by the circuit. The circuit works with a feedback mechanism. When V_D is increased, V_G (of the SET) increases. When $V_D (= V_G)$ is in region 1 (Fig. 4.15b), the $SET - V_D$ $(= FET - V_G)$ decreases and as indicated in Fig. 4.15b, we move from a $I_D - V_G$ curve at a certain V_D to the $I_D - V_G$ curve of higher V_D . But as $FET - V_G$ is lower, the MOSFET current decreases. On increasing the V_D, if the SET



(a) Effect of SET bias current (I_{BIAS}) on SF-A

(b) Effect of SET bias current (I_{BIAS}) on SF-B

Figure 4.14: Effect of SET bias current (I_{BIAS}) on SF characteristics. Increasing I_{BIAS} broadens SF oscillations, eventually flattening it out.

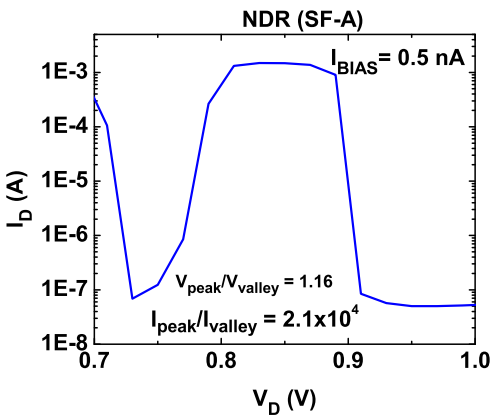


(a) **(b)**

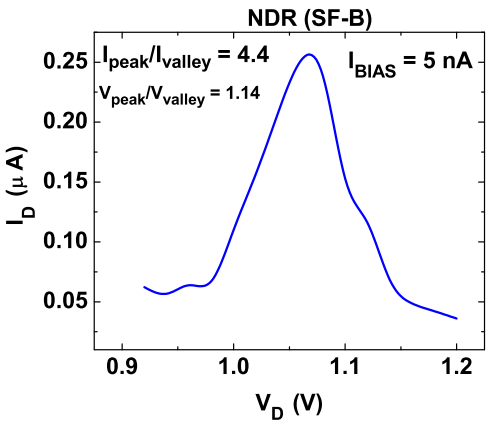
Figure 4.15: (a) Schematic of the SF NDR circuit. Here, the gate of the SET is shorted to the drain of the MOSFET. (b) Increasing V_D takes $SET\text{-}V_D$ from region 1 to 2 and then to 3. Consequently I_D first decreases, then increases and finally decreases again.

is in region 2, the MOSFET V_G increases thereby increasing the MOSFET I_D. Again when SET is in region 3, MOSFET I_D decreases as in the case of region 1. Thus NDR characteristic is obtained at the output of the circuit. NDR characteristics obtained from SF-A and SF-B are shown in figure 4.16. As SF-A output can span a large current range, extremely high peak-valley current ratio is observed in NDR circuit from SF-A. The PVCR obtained is 2.4×10^4. This is very high value compared to the range of

PVCR generally obtained with RTD (typically 10-100). On the other hand, the PVCR for NDR peak of SF-B is just 4.4. Despite being a decent value, particularly as compared to other SET based NDR devices (for eg., in ref [Inok 01b] PVCR = 2 at 27 K), it is worth noting that SET-B cannot compete with SET-A. Thus we demonstrate here the role of scaling of the SET. A higher E_C (from smaller island) will enable a high V_D operation range (about 1.1 V for SET-A), which covers the entire V_G range of the FET and hence provides high amplification, high PVCR NDR characteristics.



(a) NDR characteristics of SF-A. Extremely high peak-valley current ratio equal to 2.4×10^4 is observed.



(b) NDR characteristics from SF-B, lower peak-valley current ratio than SF-A owing to lower operating voltage of SET-B and weaker oscillations.

Figure 4.16: NDR characteristics of SF circuits.

4.3.3 SET-FET Literal Gate

The literal gate circuit, which was discussed in the previous section, is the building block of multivalued logic system. We have also seen a universal literal gate built from a SET and a FET connected in series. The functionality of a literal gate can also be obtained from the SF circuit that we have demonstrated in this section. The schematic of the circuit connections and biasing scheme used for realizing a literal gate from the SF circuit is shown in figure 4.17a. The circuit operation is qualitatively explained in figure 4.17b. In this circuit, the MOSFET is also current biased like the SET. When a MOSFET is biased with a constant current, its drain voltage goes from high to low as the gate voltage is changed from low to high value (in our case 0 to 1 V). In this

literal gate circuit, the gate of the SET acts as the input terminal (V_{IN}) for circuit. Therefore, when (V_{IN}) is increased, SET-V_D oscillates. This oscillating voltage is fed to the MOSFET gate terminal. So the drain voltage of the MOSFET (also the output of literal gate, V_{OUT}) also oscillates. Here the MOSFET acts as a rectifier producing a rectangular pulse like output. For proper rectification, the $SET - V_D$ has to be closer to the MOSFET V_T. Only then we have a 'low' output as $SET - V_D$ increases above V_T and 'high' output when it decreases below V_T.

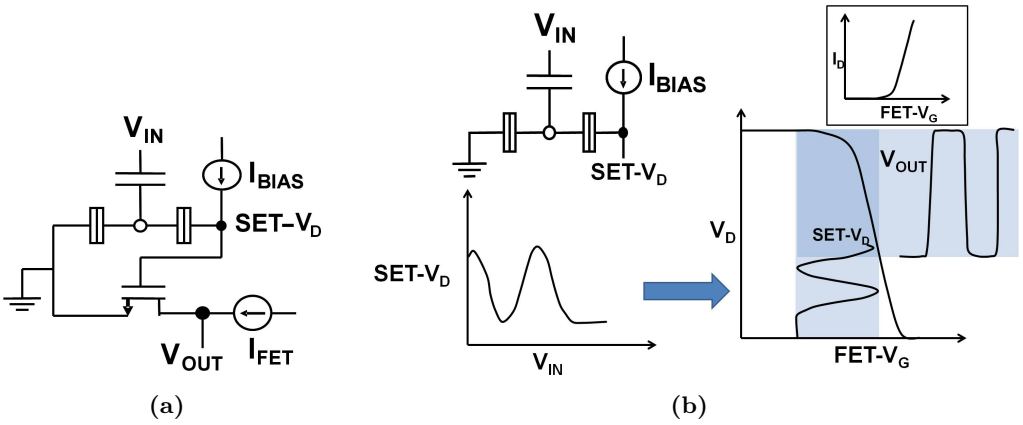


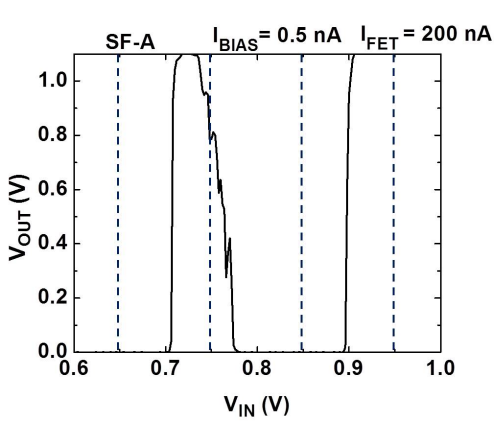
Figure 4.17: (a) Schematic of the literal gate circuit. (b) Schematic explaining the operation of the literal gate circuit.

Figure 4.18 shows the literal gate characteristics from both the SF circuits. Four bits, separated by 100 mV, can be clearly identified in literal gate from SF-A. However, the contrast between 'high' and 'low' states in SF-B literal gate output is small. So the states are not well resolved. This is due to the lower PVCR of SET-B. Therefore, high PVCR SET is necessary for obtaining well resolved bits in the literal gate (as demonstrated by SF-A, Fig. 4.18a).

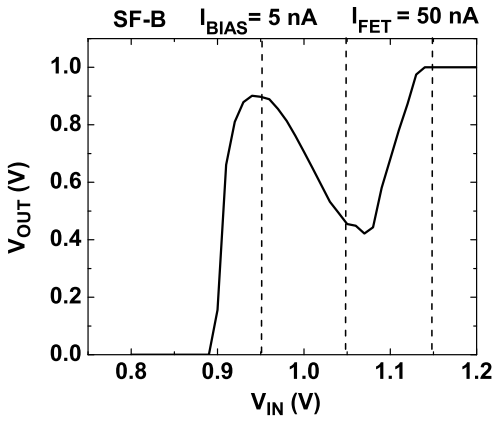
Figure 4.19 shows the effect of MOSFET bias current (I_{FET}) on the literal gate characteristics. Increasing I_{FET} increases the width of the output rectangular pulse and also improves the high to low voltage level ratio by increasing high voltage level.

4.4 Summary

To summarize, we have demonstrated various SET-FET circuits showing amplification, NDR characteristics and literal gate operation at 300 K by cointegrating a SET and a

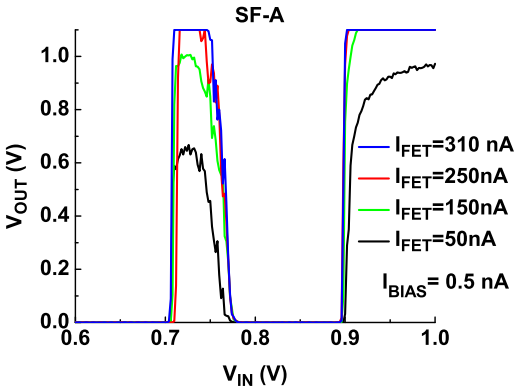


(a) Literal gate realized from SF-A. Four bits can be identified (marked as blue dotted lines) at the output for 0.65, 0.75, 0.85 and 0.95 V on the input.

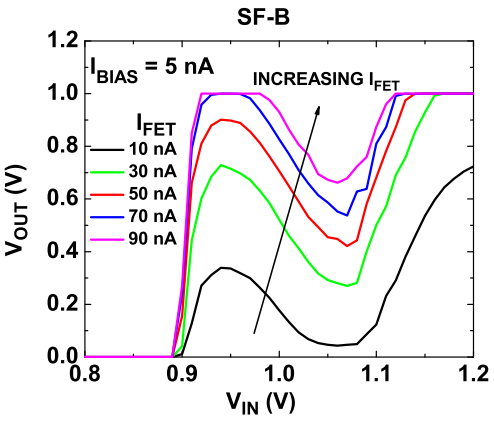


(b) Literal gate realized from SF-B. Lower contrast between 'high' and 'low' states.

Figure 4.18: Literal gate characteristics of the SF circuits.



(a) SF-A literal gate characteristics for various I_{FET} values



(b) SF-B literal gate characteristics for various I_{FET} values

Figure 4.19: Effect of MOSFET bias current (I_{FET}) on SF literal gate characteristics. Increasing I_{FET} broadens the pulse width at the output.

FET on same chip. The NDR circuit and the literal gate circuit are among the basic building blocks of multivalued memory and logic respectively. The amplifier circuit solves the problem of high output impedance of the SET. We have also demonstrated the SET scaling behavior in these circuits. A SET with smaller island (hence higher

charging energy) gives very high amplification. In fact, we have been able to demonstrate an oscillating FET due very high V_D operation of our SET (SET-A). Smaller SET also gives better figure of merit (PVCR) in the NDR circuit as compared to larger SET with lower charging energy. The literal gate performance, in terms high and low voltage state resolution, improves when size of the SET is scaled down.

5

Single Atom Transistor

In the previous chapters we have seen how a SET could be placed on CMOS roadmap to provide additional functionalities or improve certain aspects of current CMOS circuits (through SET-FET circuits) at the end-of-roadmap. In this chapter we make an effort to peep into possibilities beyond the roadmap. Here we consider Single Atom Transistor (SAT) as an ultimately scaled device with potential application in quantum computing. We discuss the possibilities of realizing a SAT in CMOS technology by scaling the MOSFET channel on SOI. We then show measurements on such scaled channel FETs that act as SATs at low temperature when the transport through them is governed by resonant tunneling through single dopant levels. We then correlate the low temperature observation of single dopant transport to the room temperature characteristics of the scaled FETs. With this correlation we show that presence of a (single) dopant in channel dramatically alters the characteristics at room temperature as compared to a device where there are no dopants in channel.

5.1 Why a Single Atom Transistor?

We have seen that the additional functionality provided by a SET still lies within the domain of current digital or analog electronics. It does not fundamentally alter the way we compute. Mutlivalued logic is an extension of binary logic to bring improvement in computing efficiency. However that is still based on computing using current or voltage levels. Recently, there has been a rising interest in bringing about a fundamental change in computing. Shrinking device sizes have brought us to a regime where quantum nature

of carriers is directly affecting device characteristics (for eg., increase of EOT by 'dark space'). Born out of these phenomena is one idea to exploit the quantum degrees of freedom of carriers to setup 'bits' for computing. This has lead to what is now popularly known as 'Quantum Computing'. Many innovative proposals have been made for realizing quantum computing in solid state systems[1]. These propose to use either charge degree of freedom [Holl 04] or spins of the electrons [Cole 05] or nuclei [Kane 98] using single dopant for a 'qbit'. Besides, the role of few or single dopants in scaled MOSFET variability is also an important issue in microelectronics [Asen 07, Akha 12]. Therefore, it is interesting to develop methods to realize devices to control and study transport through single dopant or single atom. The most basic of the devices is the Single Atom Transistor (SAT).

5.2 Transport Through a Single Dopant Level

As mentioned in previous section, the SAT is a device where in the electronic wavefunction of a dopant atom is connected by two reservoirs and additionally controlled by another electrode (the gate electrode). Dopant atom in silicon makes an ideal platform to realize this SAT scheme as it is equivalent to MOSFET geometry. A dopant in silicon has its energy level below (above) the conduction (valence) band. Therefore, the dopant is like a localized level in a barrier, as shown in figure 5.1a. In order for the carriers to tunnel through the dopant state, it has to be aligned to the Fermi level of source and drain, as shown in figure 5.1b. This can be achieved with application of a gate voltage and leads to resonant tunneling transport [Savc 95, Fowl 88, Been 91]. The magnitude of conductance in the case of resonant tunneling (G_{res}) depends on the separation between electrodes and the dopant. Transmission (Γ) of a particle (with wave vector-'k') through a tunnel barrier is given by: $\Gamma \propto e^{-2kd}$. So it falls of exponentially with barrier width d. Therefore, to have higher conductance (owing to higher barrier transmission) the barrier width should be small. In the case of a dopant in

[1]Though solid state systems are not the only contenders. There are others like cold atoms, free wave optics which are being pursued with equal interest. However, the scalability of these systems is very limited. For instance, arranging large number of cold gaseous atoms to create circuits may not possible.

MOSFET channel as shown in figure 5.1b, the transmission is given by:

$$\Gamma_{L,R} \propto \Delta exp\left(\frac{-2r_{L,R}}{a_B}\right) \tag{5.1}$$

where, $\Gamma_{L,R}$ is the transmission of the left and right barriers, Δ is the barrier height and a_B is the Bohr radius of the dopant atom (see Fig. 5.1b). The transmission decreases exponentially with increasing separation between the dopant and the electrodes (source and drain of the MOSFET).

The conductance at resonance peak (G_{res}) in the general case for a dopant in channel, when the dopant level gets aligned with Fermi levels of source/drain is given by [Fowl 88]:

$$G_{res} = \frac{4e^2}{h}\frac{\Gamma_L\Gamma_R}{(\Gamma_L+\Gamma_R)^2} \tag{5.2}$$

If the dopant atom is not well-centered and is closer to either source or drain (see Fig. 5.1c) then the peak conductance is given by:

$$G_{res} \propto \frac{e^2}{h}\frac{\Gamma_{min}}{\Gamma_{max}} \quad \text{and} \quad \Gamma \propto \Delta exp\left(\frac{-2r}{a_B}\right) \tag{5.3}$$

where, Γ_{min} and Γ_{max} are the transmission coefficients for barrier with minimum and maximum transparency respectively. r is the separation between the dopant and the farthest electrode. In order to have measurable conductance, r has to be typically less than 10 nm.

The resonant peak conductance is given in simplified terms in equation 5.4. The effect of temperature on conductance resulting from the changing Fermi distribution of electrons in the source/drain terminals is not taken into account. Considering this factor, we have for thermally broadened resonant transport:

$$G_{res} \propto \frac{e^2}{4k_BT}\frac{\Gamma_L\Gamma_R}{(\Gamma_L+\Gamma_R)^2}\frac{1}{\cosh^2\frac{e\alpha V_G}{2k_BT}} \tag{5.4}$$

This equation is valid only when $\Gamma \ll k_BT$. Notice that the conductance peak decreases in magnitude with increasing temperature.

5.3 A SAT on CMOS: Gate Length Scaling as a Way Ahead

In the previous section we have seen that we need proper coupling between the contacts and the dopant, i.e good tunnel coupling between the source/drain and the dopant. The

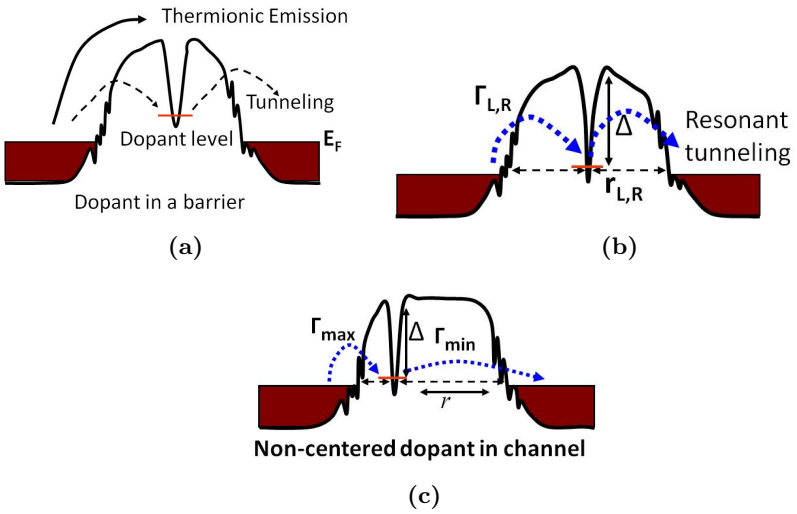


Figure 5.1: (a) Dopant level in barrier (b) Dopant level aligned to source/drain Fermi levels (c) Non-centered dopant

distance between S/D and the dopant should be on the order of 5-10 nm to have tunnel barriers with good transparency. Therefore, the net separation between source and drain should not be too high. This can be achieved by reduction of channel length, in other words with reduction in gate length and extending S/D LDD region below the gate. Thus we see that the requirement for proper functioning of the SAT is also gate length reduction which is the driving force behind CMOS scaling. Also, we see that for a functional SAT, the net channel length should be less than 10 nm. Channel length of this order are to be reached by the end-of-roadmap. So a SAT could be treated as the FET beyond the end-of-roadmap.

Another important aspect of the SAT is that the dopant level should be the major path contributing for conductance through the transistor. Ideally it has to be the only channel for transport. Therefore transport over the barrier or direct tunneling from source to drain should be reduced. This could be done by reducing the barrier area. Since the barrier in this case is the channel potential barrier in OFF state, this amounts to reduction of channel width. This is in-line with MuGFET scaling for next CMOS nodes.

These two factors support and motivate the development of the SAT on CMOS technology. Its development would be synergic to scaled MOSFET development and would be an addition to CMOS device technology when roadmap end is reached!

Development of the SAT has more challenges than development of scaled MOSFETs with gate length reduction. The major challenge for building an efficiently functional SAT is the deterministic placement of a single dopant in the channel. Best known method today is scanning tunneling microscope (STM) based deterministic placement of single dopant on silicon surface pioneered by research group at UNSW [Scho 03]. It is a combination of hydrogen resist and STM lithography [Lydi 94]. The silicon surface is first passivated with hydrogen. Then using STM, hydrogen bonds are selectively dissociated to form patterns. It is then annealed in Phosphorus gas. The hydrogen passivation acts as a mask and P atoms attach to silicon only in places where H atoms have been removed. Thus atomistic precision in dopant atom placement is achieved. This method has been used to successfully fabricate a SAT recently [Fuec 12]. But this method is highly limited in terms of scalability. As individual dopants have to be placed on silicon surface using STM tips, it would require millions of such tips to fabricate millions of SATs on a single chip on a commercial scale. Also, up to now the source/drain contacts and the gate have also been formed by larger P doped regions through the same process. Therefore it largely increases fabrication time as hundreds of H atoms have to be dissociated to form source, drain and gate electrode regions. Though this method is an excellent approach to demonstrate proof-of-concept SAT based devices, but the excellent control on placement of dopants comes at a cost of throughput and scalability.

Another notable method has been the single ion implantation in nanowire Si channels using low energy ions [Shin 02, Mats 97, Weis 08]. Considerable progress has been made by several groups in deterministic placement of dopants by implanting and detecting ions in the channel one-by-one[Shin 05, Tan 10, John 10]. However, the dopant placement is still limited by staggering of ions in the silicon lattice [John 10] and atomic level precision is challenging. Additionally it is also required to develop a robust method for in-situ detection of single ions during implantation. This method of single ion implantation is very interesting as it relies on classical ion implantation technique and could be integrated into CMOS process without considerable challenges.

Therefore it is also equally interesting to study single dopant present in the channels of state-of-the-art CMOS devices. Scaled MOSFETs with isolated single dopant in channel can also compete as good option at present to realize a SAT. Since the SAT will be based on very mature CMOS technology, ever progressing CMOS technology

will benefit the SAT considerably in future. In current CMOS technology, we propose to utilize the FDSOI MOSFET device architecture to realize a SAT. In this technology the channel is undoped. But since the S/D formation is done through ion implantation and dopant activation by annealing, we can aim at exploiting few dopants diffusing into the channel for realizing a SAT [Pier 10b]. Also, by reducing channel width we can effectively suppress multi-dopant presence in channel and statistically increase the probability for single dopant presence. Another option could be to moderately dope the channel, to a doping of about 1e18 cm^{-3} (dopant type same as S/D). This would be equivalent to 1 dopant per 10×10×10 nm^{-3} of silicon (for 10 nm width and 10 nm channel length). Besides, we can considerably improve the control on one dopant with use of more gates (including the substrate as back-gate) and 'tune' into the energy window of that single dopant. Therefore, keeping the conventional FDSOI-MOSFET integration scheme and scaling channel lengths to 10 nm and below, we can realize SATs that can be experimental testbed to study and develop our understanding of single dopant devices.

The devices used in this thesis for studying single dopant transport are ultrascaled nanowire channel FDSOI MOSFETs with high-k/metal gate. The typical gate length, L_G is about 15 nm and the width of the nanowire channel is about 65 nm.

5.4 Transport Through a Single Dopant at Low Temperature: Formation of a SAT

At low temperature (4.2 K and below) all the thermally activated transport over the barrier is suppressed. So the sole contribution to conductance will be due to tunneling through the dopant state. Therefore we first show low temperature measurements of the scaled channel nanowire MOSFETs. Low temperature measurements are done again with a lock-in system as described in section 3.3.2. We have also made use of the substrate of SOI wafer as 'back gate' in some measurements. Since the substrate of industrial SOI wafers has very low doping (about 10^{15} cm^{-3}, p type), carriers freeze out at low temperature. So changing the substrate voltage becomes very difficult as it has very slow relaxation time (on the order of days). Therefore we shine light on the device to induce some carriers in substrate. With increased carrier concentration the substrate conducts good enough to follow the applied back gate potential reasonably fast. This

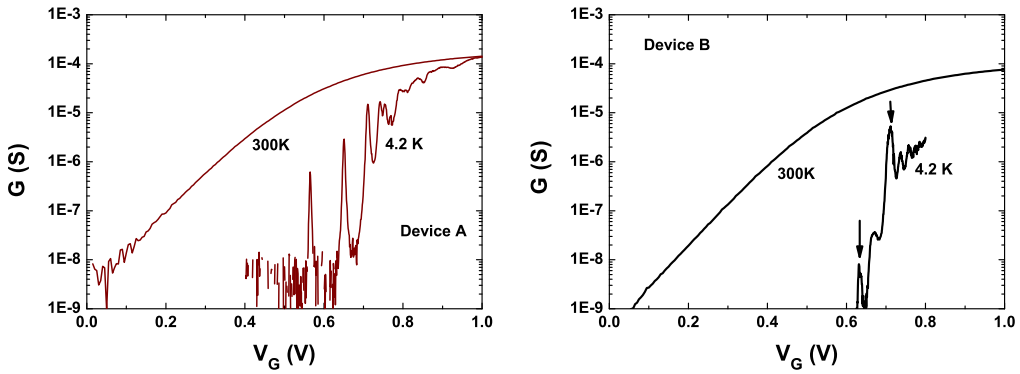
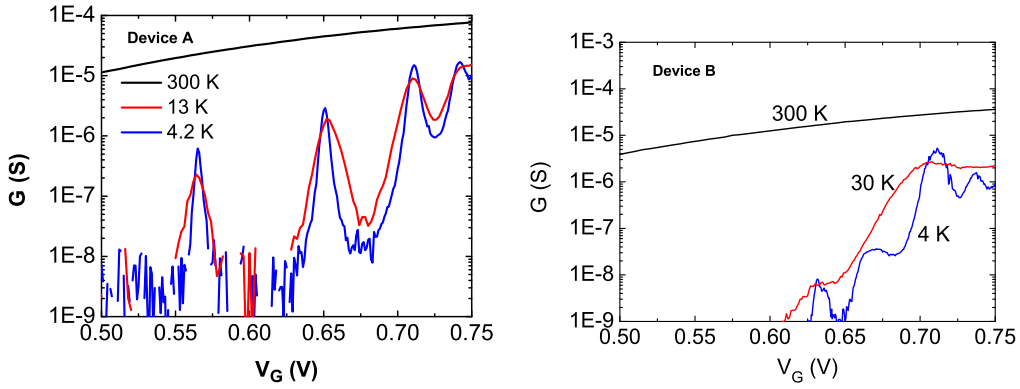


Figure 5.2: (a) $G - V_G$ at 300 K and 4.2 K for device A. Strong dopant resonances are observed at 4.2 K. (b) $G - V_G$ at 300 K and 4.2 K for device B. Dopant peaks marked by arrow.

is done through a LED anchored at 4.2 K. LED is only switched on briefly when substrate voltage is changed. This method works very efficiently and has enabled us to demonstrate SET to FET transition at low temperature in underlap devices [Roch 12b].

Figure 5.2 shows $G - V_G$ plots for two devices, A and B. They have the same nominal dimensions. The $G - V_G$ curves are measured at two different temperatures: At 300 K and at 4.2 K. Both devices show classical FET behavior at 300 K. Device A (Fig. 5.2a) when cooled down to 4.2 K, shows well resolved, sharp peaks at V_G = 0.565 V and 0.65 V. These peaks are attributed to thermally broadened resonant tunneling transport through the dopants. We suppose that each peak corresponds to one dopant atom, which will be discussed in more detail later in this section. The peaks have considerably good conductance (7×10^{-7} S and 3×10^{-6} S) as compared to the quantum conductance (4×10^{-5} S) indicating that the barriers on either side are equally transparent. Hence we suppose that these dopants are well-centered in the channel. On the other hand, device B also shows peaks at 4.2 K (marked by arrows). But these are not so sharp and well resolved as compared to A. Also, the conductance of the first peak at V_G = 0.63 V is very low. This is due to one of the barriers being more resistive. Hence we suppose that in this case the dopant is not well-centered.

Figures 5.3a and 5.3b show evolution of the peaks in device A and B at intermediate temperature (between 300 K and 4.2 K). It is seen in both devices that the peaks broaden with increasing temperature and also the peak conductance drops down. This



(a) (b)

Figure 5.3: (a) $G - V_G$ at different temperatures for device A. Temperature evolution of $G - V_G$ curves indicates resonant tunneling transport (b) $G - V_G$ at different temperatures for device B. Resonant tunneling transport is evidenced in temperature evolution of $G - V_G$ curves

is a signature of resonant tunneling transport. Such an evolution of $G - V_G$ curves with temperature is expected in the case of resonant tunneling through a single level [Savc 95, Been 91]. Thus we confirm that the peaks correspond to resonant transport through the dopant levels.

Finite DC V_D bias conductance 2D plot of the peaks in A is shown in figure 5.4. Here we still measure the differential conductance with a lock-in and a small ($\ll k_B T$) AC excitation, but additionally we also apply finite DC bias across the source and drain terminals. This enables us to measure conductance in non-linear regime. Two diamonds are measured for the first two peaks. From the slopes of the first diamond in the figure, we deduce the coupling of the dopant level with S/D electrodes. These are given by:

$$\frac{C_D}{C_G} = 0.9 \quad \text{and} \quad \frac{C_S}{C_G} = 1.27 \tag{5.5}$$

The coupling ratios are nearly the same for source and drain (with slightly higher coupling with source), indicating that the dopant is well centered in the channel. The lever arm factor for gate coupling can be calculated as:

$$\alpha = \frac{C_G}{(C_G + C_D + C_S)} = \left(\frac{C_D}{C_G} + 1 + \frac{C_S}{C_G}\right)^{-1} = 0.24 \tag{5.6}$$

This value is small. However, it is larger than the value obtained in similar single dopant device ($\alpha = 0.16$) in ref [Pier 10b]. It is coherent with the fact that as compared

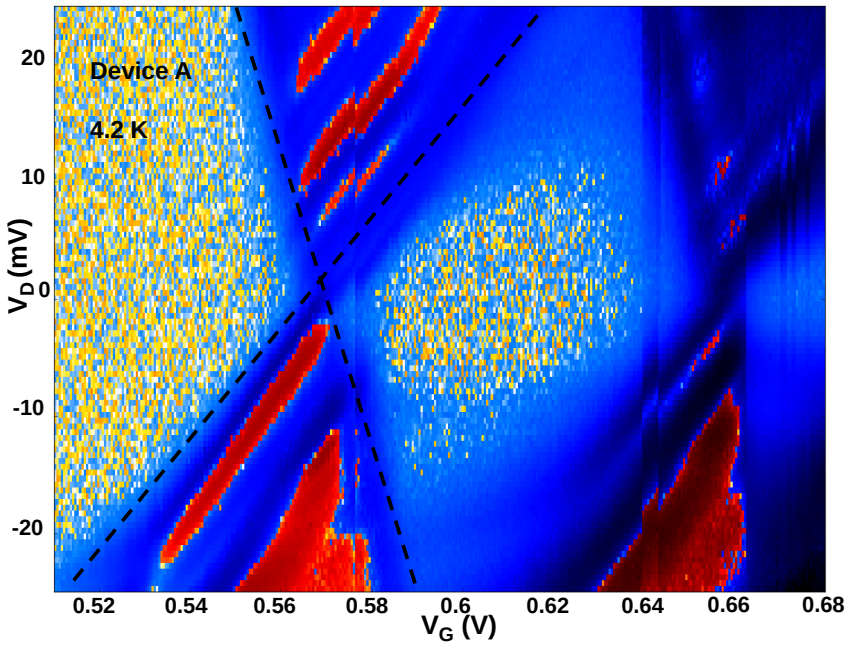


Figure 5.4: Differential conductance plot as function of V_G and V_D for device A.

to device in ref [Pier 10b] which had thicker gate oxide (5 nm SiO_2 and higher silicon thickness (20 nm), the device A has lower Si thickness (8 nm) and smaller EOT (about 1.8 nm). So we observe better control of the channel by the gate. It will be seen that this becomes an important factor in analyzing 300 K characteristics of such devices, which will be discussed in the next section.

Also, one can notice lines of negative differential conductance (red color) running parallel to the diamond edges. These lines are due to local density of states fluctuation in source or drain terminals. It is indication of atomistic nature of the contact edges as only few dopants are present at the end of S/D extensions [Pier 10a]. Note that there are no lines running parallel to diamond edges towards higher V_G direction. So we do not see transport through excited states for the first dopant and no lines of co-tunneling in the diamond as observed in ref [Pier 10b]. So the two peaks in $G-V_G$ curve (Fig. 5.2a) are supposed to be transport through two different dopants.

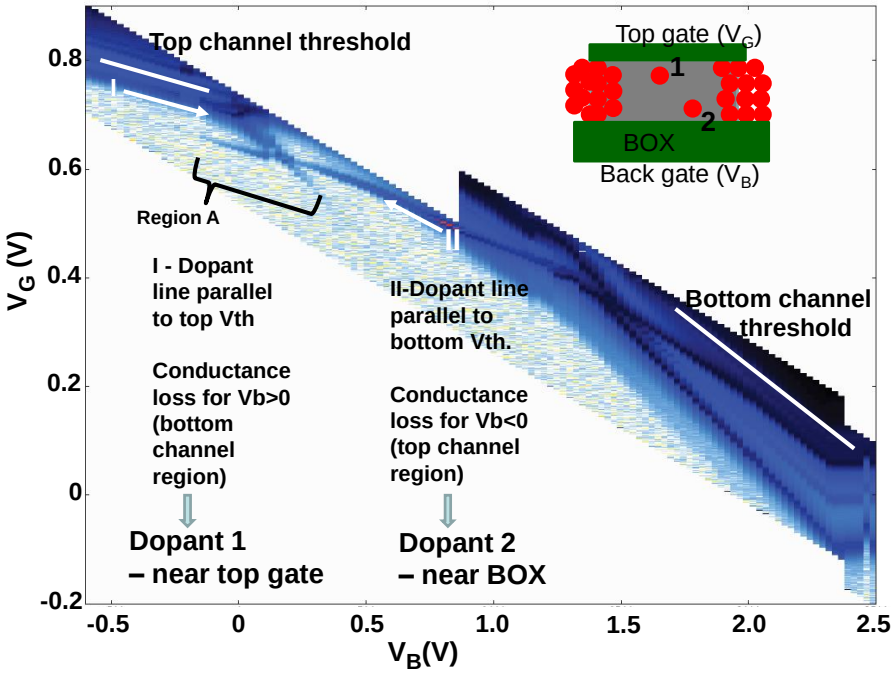
5.4.1 Determination of Vertical Position of Dopant

It has been found out that the vertical position of dopants in silicon (between gate oxide and BOX interface) leads to different effects such as increase in ionization en-

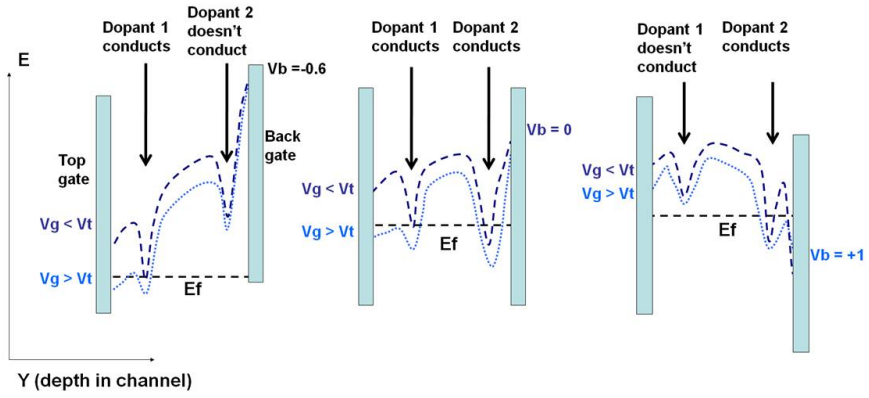
ergy [Pier 10b] or hybridization with surface channel [Lans 08]. These might have different effects on the SAT based computing schemes as the theoretical proposals do not take into account the formation of 2DEG at the surface or the electric field, dielectric environment of the dopant closer to surface. Vertical positioning in the silicon can be identified using coupling with the back interface [Khal 07]. This is done by studying the evolution of dopant peaks with back gate voltage. Another important application of the back gate is also the ability to tune coupling of dopants with electrodes or with other dopant energy levels [Roch 12a]. The position of dopant peak in V_G indicates the energy of the level. Dopant with highest ionization energy (one near BOX in ref [Pier 10b]) has a peak at lowest V_G. Evolution of $G - V_G$ with back bias (V_B) is given in figure 5.5 as a 2D plot for device B. The dopant peak evolves with V_B as a line parallel to the inversion channel corresponding to the interface it is closer to. As seen the two dopant peaks observed at $V_B = 0$ come from one dopant near BOX and one near topgate. The first peak is from the dopant near BOX, confirming increase in ionization energy. We also see two other lines crossing around $V_B = 1.5$ V and $V_G = 0.35$ V. This may be the feature due to capacitive coupling of two dopants as observed in ref [Khal 07]. But the resolution of measurement in figure 5.5 is not sufficient to conclude if it is indeed a feature from coupled dopants (similar to coupled dots [Wiel 02]).

5.5 Room Temperature Characteristics: Impact of A Single Dopant

In the last section we have shown transport through single dopant in sub-15 nm channel MOSFETs at low temperature. In this section we show the effect of these dopants on the room temperature characteristics of these devices, by comparing them with a device where there are no dopants in the channel. Impact of few dopants on ultra-scaled MOSFETs, termed Random dopant fluctuation (RDF), has been considered as one of the major source of variability [Asen 07] particularly in bulk technology. But the nanowire MOSFETs studied in this work have fully depleted architecture with undoped channels. Thus they offer intrinsically improved variability [Webe 08]. However, in sub-15 nm channel devices the issue of concern comes from diffused dopants from source/drain extensions. This intrinsic variability coming from S/D diffused dopants



(a)



(b)

Figure 5.5: (a) 2D plot of $G - V_G$ for various V_B (back bias) for device B. Two dopant lines (I and II) run parallel to top channel threshold and bottom channel threshold resp (marked by white arrows). Dopant line I fades off as V_B goes positive i.e. as back channel conduction starts. II follows opposite trend. It fades off as V_B goes negative i.e. as front channel starts. As shown in band diagrams (b), line I comes from a dopant near top gate as it conducts when top channel dominates and line II comes from a dopant near BOX as it conducts when bottom channel starts conducting

is generally characterized by measuring V_T difference resulting from source/drain commutation [Sugi 10] (estimating V_T, once with source, drain in normal configuration and once with S/D reversed). This method gives source-drain asymmetry. But this method can not estimate impact of few dopants or down to single dopant level. Our group experimentally demonstrated impact from single dopant in ref [Wacq 10]. Figure 5.6 (taken from ref [Wacq 10]) shows the Kinetic Monte Carlo simulation (KMC) results for diffusion of dopants into the channel taking into account activation annealing and all the thermal budget involved after dopant implantation. It can be seen the few dopants diffuse and reach the middle of the channel. Additionally, it was also shown that one of these dopants with strong tunnel coupling to source and drain lead to degraded MOSFET characteristics at 300 K. But the devices in ref [Wacq 10] were experimental devices and far from devices of current FDSOI technology. Here we experimentally

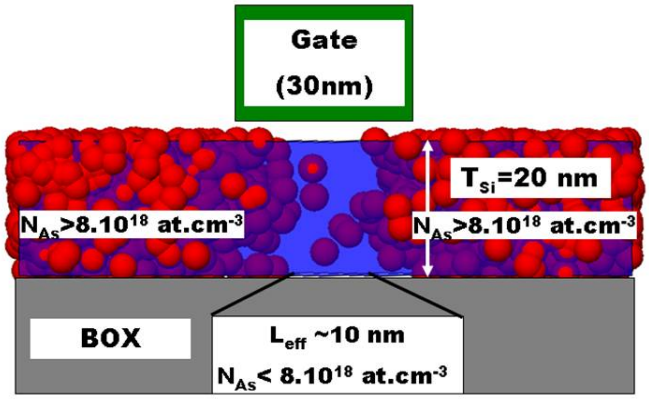
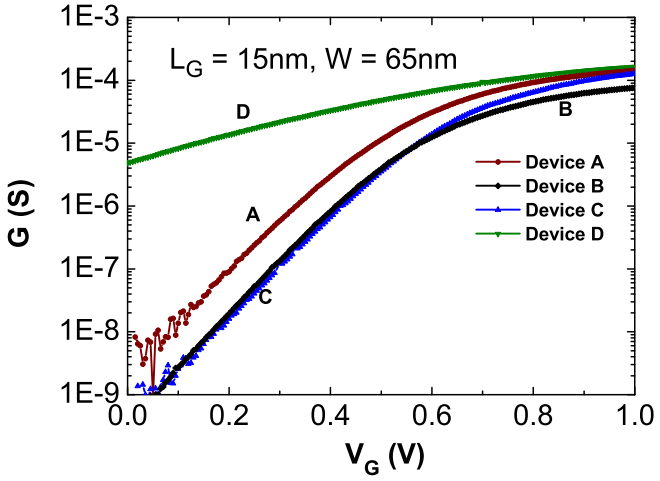
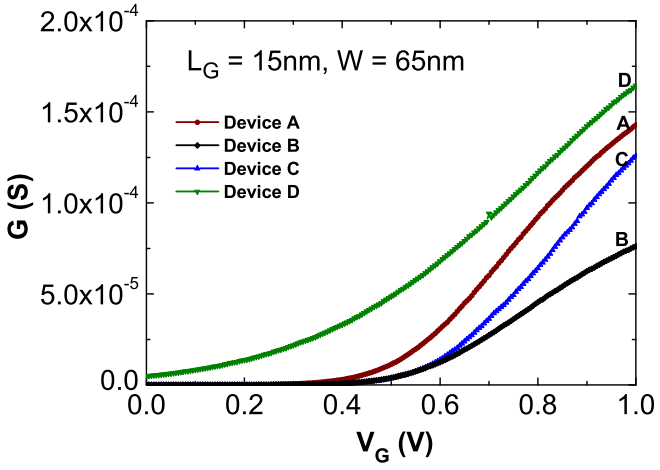


Figure 5.6: Kinetic Monte Carlo (KMC) process simulation showing diffusion of dopants into the channel after annealing and other thermal process involved in fabrication. Each red sphere is an As dopant at the Bohr radius scale. As seen dopants are likely to reach the middle of the channel. Figure from [Wacq 10].

study the single dopant impact on devices on current FDSOI technology developed at LETI. Also for the first time we show impact of single dopant on substrate biasing at 300 K. Figure 5.7 shows the $G-V_G$ plots of four nominally identical devices with $L_G =$ 15 nm, W = 65 nm that span the entire spread of characteristics. Devices are chosen as representative of the effects that produce the variability. Along with device A and B (discussed in previous section), the graph shows two more devices labeled C and D. Notice that B and C have roughly the same V_T but different G in ON state(Fig. 5.7). $G - V_G$ measurements of device C down to 4.2 K are shown in figure 5.8. There are



(a)



(b)

Figure 5.7: (a) $G - V_G$ plots in log scale for 4 nominally identical devices with L_G = 15 nm, showing the spread of device characteristics below threshold. (b) $G - V_G$ plots in linear scale for 4 nominally identical devices with L_G = 15 nm, showing the spread of conductance in ON state.

no resonant tunneling peaks in device C $G - V_G$ curve at 4.2 K. Therefore, we suppose that there are no dopants well-connected to source/drain in the channel of device C.

Having confirmed that device C does not have dopants in its channel, we take it as a reference and compare the room temperature characteristics of device A and B with that of C. As seen in figure 5.7a, device B and C have nearly the same V_T. But their ON state conductances are not the same (Fig. 5.7b). The presence of dopants (Fig. 5.3b) alters

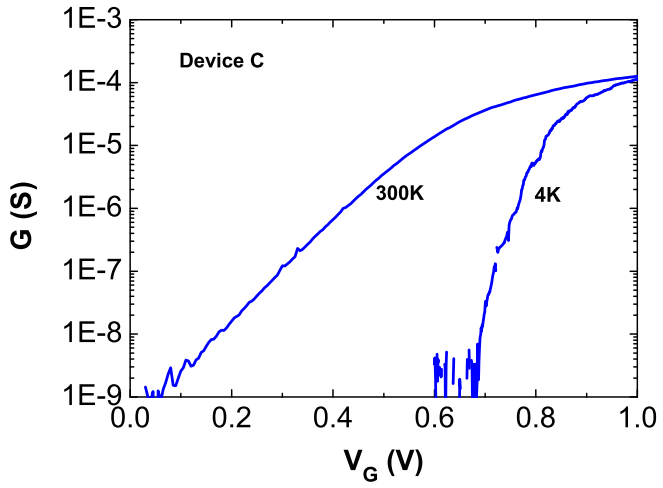


Figure 5.8: Evolution of $G - V_G$ with temperature for device C. No dopant peaks are observed.

'I_{ON}' of B with respect to C, indicating RDF effect on I_{ON} as previously suggested in simulation studies [Besc 10]. This is believed to be due to enhanced Coulomb scattering by the dopants.

Now comparing, device A and C, we see in figure 5.7a that device A has substantially higher leakage at room temperature in comparison to C. This due to lower V_T of device A as compared to C. We have seen (Fig. 5.2a) that device A has two well-centered, well-coupled dopants (manifested by their high peak conductance) in its channel. Therefore these dopants substantially impact the subthreshold leakage in the device at room temperature leading to reduction of V_T in comparison to C. Major contribution to increased subthreshold current at 300 K in device A comes from the thermally broadened resonant transport through these dopant states. However, no impact on subthreshold slope (SS) is observed. As there are no dopants that contribute to leakage for very low V_G values (absence of dopants with energy level aligned to S/D Fermi level, E_F, for $V_G = 0$ to 0.5 V) the SS is not degraded as in ref [Wacq 10].

Fig 5.9 shows V_T values for various VB (back biasing) for devices A, B and C at 300K. V_T modulation by V_B changes considerably due to dopant presence. Again we consider device C as reference and the V_T evolution with V_B as normal behavior. Comparing with C, device B shows slightly degraded control of V_T by V_B. But for A, V_T modulation by V_B is negligible. This shows the difficulty to reduce leakage in case of well coupled dopants.

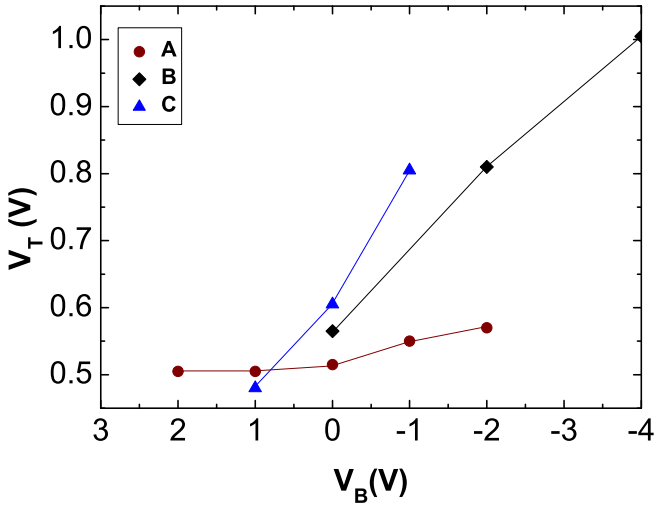


Figure 5.9: Change of V_T with V_B for devices A, B and C at 300 K. B and C have close dependence as a function of V_B whereas it is almost negligible for A. It shows difficulty to reduce leakage in case of well coupled dopants.

As a summary, we evidenced that the presence of few diffused dopants (or even one) dramatically alters the electrical characteristics when channel lengths around 10 nm are reached.

Measurements on device D are presented in figure 5.10. Device D has a highly degraded SS and very low V_T similar to a single dopant dominated device as in ref [Wacq 10].

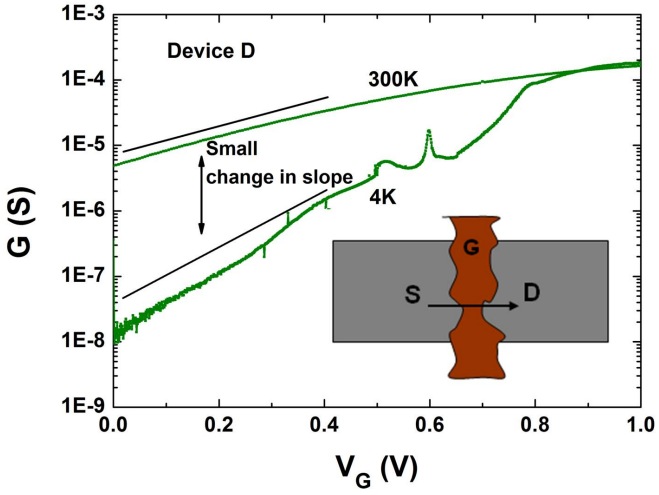


Figure 5.10: $G-V_G$ at different temperatures for device D. Very small dependence of SS on temperature is a clear signature of source-drain direct tunneling due to L_G reduction.

However, notice the strikingly distinct evolution with temperature. The SS undergoes a very small change with temperature. This high leakage nearly independent of T is due to direct source to drain tunneling and results in very high I_{OFF} at room temperature. This effect occurs when channel lengths are less than 10nm [Stae 02, Loli 04] and represents one of the fundamental limits on MOSFET scaling.

5.6 Summary

In this chapter we have demonstrated formation of a Single Atom Transistor (SAT) at low temperature in sub-15 nm channel length nanowire MOSFETs. This was done by studying the transport through a single dopant that had diffused from source/drain into the middle of the channel. Resonant tunneling transport through the dopant levels were observed and transport through single dopant was further confirmed by measuring differential conductance in non-linear regime. This observation of resonant tunneling through dopant state was possible due to scaled channel length in our devices that allowed a good overlap of dopant electronic wavefunction with source/drain electrodes. Thus we demonstrated gate length scaling as an option to realize a SAT in CMOS technology. Adding more gates on the nanowire channel (which is readily possible in CMOS fabrication) we can have greater control on a dopant and also on its coupling to other dopant's energy levels and also with the electrodes. Therefore it would enable one to realize some of the single dopant based quantum computing schemes, where such couplings are essential to create circuits.

6

Conclusions and Perspectives

6.1 Conclusions

In this work we have demonstrated a single integration scheme for realizing ultrascaled trigate nanowire MOSFETs (NW-MOSFETs)and room temperature operating Single Electron Transistors (RT-MOSSETs)on SOI. This is the first effort wherein a room temperature operating SET has been realized in a semi-industrial CMOS foundry on 300 mm wafers which are current industry standard. The NW-MOSFETs realized alongside the MOSSETs have characteristics that are on par with the requirements of ITRS for the next generation CMOS nodes. The electrostatics are among the best reported for trigate MOSFETs down to 20 nm gate length. This synergic development of RT-MOSSETs and NW-MOSFETs on a single platform marks a considerable progress for the SET technology. This is the main highlight of this work in comparison with many of the previous efforts on Si based RT-SETs and in a way demonstrates *coming of age* for the SET.

The main advancements and contributions of this thesis can be summarized as follows:

- We demonstrated room temperature operating SET (RT-MOSSET) and ultrscaled NW-MOSFETs with L_G down to 20 nm through a trigate nanowire geometry with width down to 5 nm. A single integration scheme (section 3.2) is developed to realize these two kinds of devices simultaneously. The integration scheme features current generation high-k/metal gate stack. It is also the first demonstration of

RT-SET with high-k/metal gate and thus demonstrates complete integration of SET in the CMOS technology.

- Scaled NW-MOSFETs with width = 7 nm show $DIBL$ = 12 mV/V and near ideal SS = 62 mV/dec for a gate length L_G = 20 nm. A transition from FET to SET behavior is observed in 5-7 nm width nanowires at room temperature. This transition enables realization of RT-MOSSET (section 3.3).

- We propose that the transition originates from disorder induced localization of carriers in 5-7 nm width nanowires. One major source of this disorder is the surface roughness of the nanowires. Localization creates small islands and tunnel barriers in the nanowire. Thus we observe RT-MOSSETs with very high charging energy, with operating voltage as high as ±0.9 V! This is not only among the highest operating voltage ever reported for SET but also corresponds to current generation CMOS voltage level. Therefore it shows that the SET can be treated on same footing as the MOSFET easing cointegration from circuit design perspectives.

- As a demonstration of the prime advantage of our integration scheme, we have shown SET-FET hybrid circuits with various functionalities (section 4.3.1) at 300 K, cointegrated on same chip. Benefiting from high operating voltage of our RT-MOSSETs we achieved SET current amplification to milliampere level with a dynamic range ($I_{ON} - I_{OFF}$ ratio) more than 4 orders in magnitude. SET-FET hybrid circuit with negative differential resistance (NDR) characteristics (PVCR $> 10^4$) was also demonstrated. Literal gate circuit having multi-bit output was also realized. Besides, we also showed impact of charging energy on these circuits by using two SETs with charging energies differing by almost one order of magnitude.

- We realized a Single Atom Transistor (SAT) on CMOS platform by scaling the channel length down to 10 nm. Low temperature transport measurements showed resonant tunneling transport though a single dopant. We further investigate the vertical positioning of the dopants in the channel by measuring relative coupling between top gate and back gate (substrate). As an additional benefit of our study, correlating low temperature and room temperature transport measurements, we

were able to demonstrate impact of single dopant on room temperature characteristics of current generation FDSOI MOSFETs fabricated at LETI.

6.2 Perspectives

Here, perspectives for this work are mentioned based on the knowledge and experience gained by the author during the period of the thesis work. Our RT-MOSSETs are fully fabricated in CMOS technology that is very close to process flow widely used in industries today for current generation MOSFETs. However, many challenges remain and there is lot of room for improvement. In terms of the MOSSET integration and in general for the combined MOSSET-MOSFET technology platform, we would like to propose the following paths for further progress:

- The main challenge is the stochastic nature of the RT-MOSSETs. As they are formed by disorder potential of nanowires, naturally their characteristics will be stochastic. This is challenging for realizing large scale integrated circuits from the SETs. There is need for improving the integration scheme to realize well controlled RT-SETs with less variability. One possible method to achieve this to use hydrogen annealing to smoothen the nanowires after etching. This will reduce the disorder and lead to controlled island that corresponds to channel dimensions.

- Realizing controlled and reliable tunnel barriers is also equally important for a SET technology. Moreover, it should be possible to form these tunnel barriers selectively only for SETs in a SET-FET cointegration scheme. Since doping underlap may not be sufficient to confine electrons at room temperature, 'counter doping' for LDD extensions could be used, i.e. using 'p' type LDD region with n-type source/drain regions. But it should be noted that uniformly doping very small width nanowire ($\sim$5 nm) nanowire below spacers can be a significant challenge. In this respect, Schottky barriers formed by silicidation can also be an encouraging option.

- It is also necessary to have TCAD simulation platform to simulate the SET. Going further on the lines of NEGF based simulations (section 3.4.1), an *ad hoc* scheme can be developed to include Coulomb blockade. Carrier density in the channel, barrier transmission, and potential along the nanowire can be extracted

along a plane in the transport direction for each gate voltage step. Using this information, 1D transport simulation using master equation can be performed. Though not self-consistent, it could still give qualitative estimation of the SET characteristics for the device design under consideration.

- In terms of SET-FET based circuits, there is need for a realistic SET compact model that sufficiently accounts for RT-MOSSET characteristics. Most of the compact models developed until now are based on orthodox theory and fail to simulate RT-MOSSET characteristics. A good compact model will enable realistic simulation of SET-FET circuits and also in quantifying the *real* power advantage offered by SET. As popularly claimed, SET as a low power device is not straight forward. It largely depends on the nature of the SET based circuits. Considering recent progress and current improvement in low power segment of CMOS technology, it is all the more essential to exactly quantify SET-based circuit power consumption.

- On the physics side, further characterization of the RT-MOSSETs under magnetic field will be an interesting study. Also, as the SET offers potential for highly sensitive charge detection (as a radio frequency-SET) experiments have to be designed and performed specifically adapted to get best sensitivity from high temperature operating SETs (having high output impedance).

Factors discussed above were mostly concerned with the technical aspects of the SET. On a more general note, it is difficult and risky to be *predictive* about the general future of the SET and the SAT. Clearly, integrating the SET on state-of-the-art CMOS technology eases considerably the skepticism from the CMOS industry about its practical feasibility. But there are other factors that also greatly impact if at all the SET will ever make it into commercial devices. One of them is the additional functionality offered by the SET with respect to the current CMOS and the corresponding cost advantage. The SET-FET hybrid circuits for analog applications certainly look one encouraging area. Innovative circuit schemes (especially in analog applications) are required to truly push the SET into mainstream ICs. In the rapidly changing and progressing CMOS world, now it looks realistic that we will see the MOSFET scaling till the actual physical limits are reached. Beyond that, as shown in this work, the MOSSET comes about naturally on the roadmap. Smart integration of the MOSSET

with the scaled MOSFET without higher cost overheads might actually bring the SET into commercial scenario.

The SAT on the other hand has rather a long way to go before one could talk about practical circuits. However, it is a great experimental test-bed to study quantum phenomena at the atomic scale in solid state devices. The phenomena unraveled through these experiments will definitely add a great deal to our knowledge and will play immense role in future if and when quantum computing is realized.

Appendix A

Appendix

A.1 Nanowire CD-SEM Measurement

Measurements for determining the width of nanowires were carried out in an in-line automated CD-SEM tool. 18 dies were measured covering all quadrants of the wafer: 9 dies after lithography and 9 adjacent dies after etching as shown in figure A.1. It is well known that e-beam observation changes CD (critical dimension) of the observed resist patterns (patterns after lithography) and so we choose adjacent dies for observation after etching, as they are free from this resist CD modification.

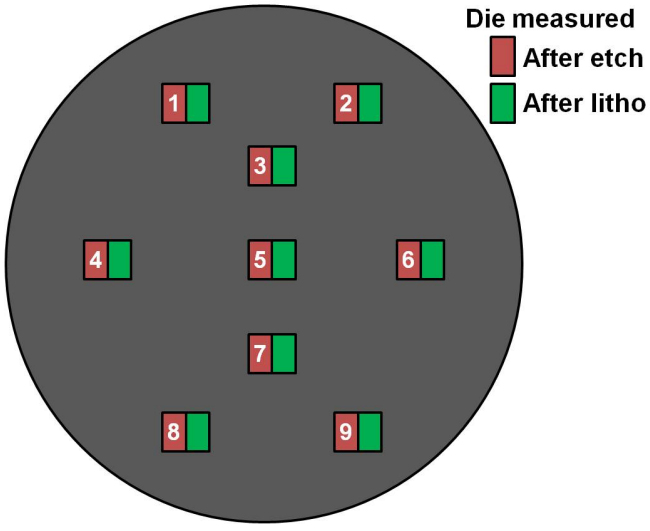


Figure A.1: Schematic showing dies measured with CD-SEM.

When width of a pattern is measured, the measurement is done on 32 points in a

Table A.1: CD-SEM measurement statistics on whole wafer.

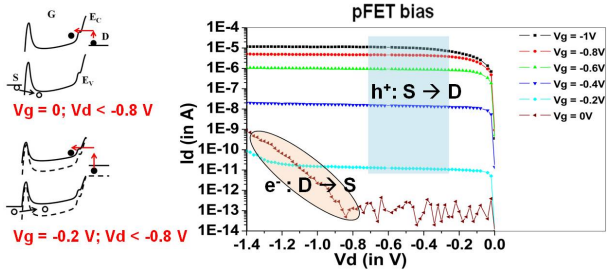
Die number	Single Nanowire width (nm)	Nanowire in Array (nm)
1	7.9	18.87
2	7.54	18.04
3	7.94	20.51
4	7.62	19.42
5	5.21	17.79
6	7.23	20.03
7	7.95	21.02
8	7.54	20.24
9	6.82	20.72
Max	7.95	21.02
Min	5.21	17.79
Mean	7.31	19.63
Max-Min	2.74	3.23
3σ	2.6	3.51

chosen region of the pattern (in our case nanowire) and then they are averaged to get the width. Measurements for single nanowire and nanowire array are given table A.1.

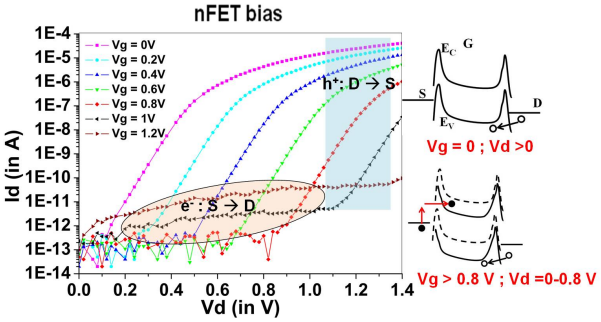
It can be seen that for the same trimming process, single nanowires have smaller width compared to nanowires in array.

A.2 Ambipolarity Analysis for Schottky Devices

The Schottky MOSFETs under study in this thesis have dopant segregation at the Schottky interface (Silicon-silicide interface). Therefore it is important to ascertain that the Schottky nature of the source/drain to channel junction is still intact. Excess doping at interface turns silicide-silicon junction into ohmic type thereby making the devices conventional doped source/drain-like where transport is governed by source-channel p-n junction depletion region instead of the Schottky barrier. This is checked for by ambipolarity analysis [Huti 09]. Figure A.2 shows biasing of the PMOSFET both in pFET and nFET configuration respectively. It can be clearly seen that both cases the drain current (Id) - drain voltage (Vd) curves show transistor characteristics indicating ambipolar nature of the device.



(a)



(b)

Figure A.2: Measured Id-Vd curves for Schottky PMOSFETs in both pFET (Vg<0,Vd<0) and nFET (Vg>0,Vd>0)configuration. Schematic of band diagrams are shown for qualitative understanding of carrier injection at various bias values. (a) pFET biasing scheme. At Vg=0V, current due to the Thermionic-Field Emission (TFE) of electrons from D to S is seen at high Vd. This confirms ambipolar behavior. (b) nFET biasing scheme. At high Vg and low Vd values, current plateau due to tunneling of electrons from S to D is visible.

Additionally plateaus are seen in Id-Vd curves in both biasing schemes. In pFET configuration (Fig. A.2a) at Vg=0 V and high Vd (>0.8 V) current starts rising due to thermionic field emission (TFE) of electrons from drain (D) to source (S). On decreasing the Vg to -0.2 V in addition to this, the current at low Vd increases due to increases S to D hole current Similarly, in nFET configuration for Vg>0.8 V and low Vd (0-0.6 V) current plateau is seen due to tunneling of electrons from source to drain. Thus these measurements demonstrated transport of both type of carriers in the device. Therefore, the ambipolar nature of the device is confirmed and it can be concluded that the junctions are governed by Schottky injection.

A.3 Measurement Setup for SET-FET Circuits

As mentioned in chapter 4, the fabrication of our wafers was stopped at M1 level. Therefore, we did not have the different devices connected on the chip through metal lines. In order to make circuits (SET-FET circuits) we had to connect them externally. Typical connections we made to realize SET-FET circuits are shown as a simplified schematic in figure A.3. We chose the die with the SET under study. On the same die we also have wide planar FET, which will be coupled to the SET. The SET and FET are in different areas of the die. Typical die size is about 1.5 cm×1.5 cm. All the measurements are carried out on 300 mm wafer with wafer placed in standard probe station. Probes are then placed on respective SET (and FET) source, drain and gate pads. To realize required shorts between different terminals, a connector board with 'T' section is used. The connector board also connects the terminals to SMUs of the semiconductor parameter analyzer. The current mode setting in the parameter analyzer is used for current biasing.

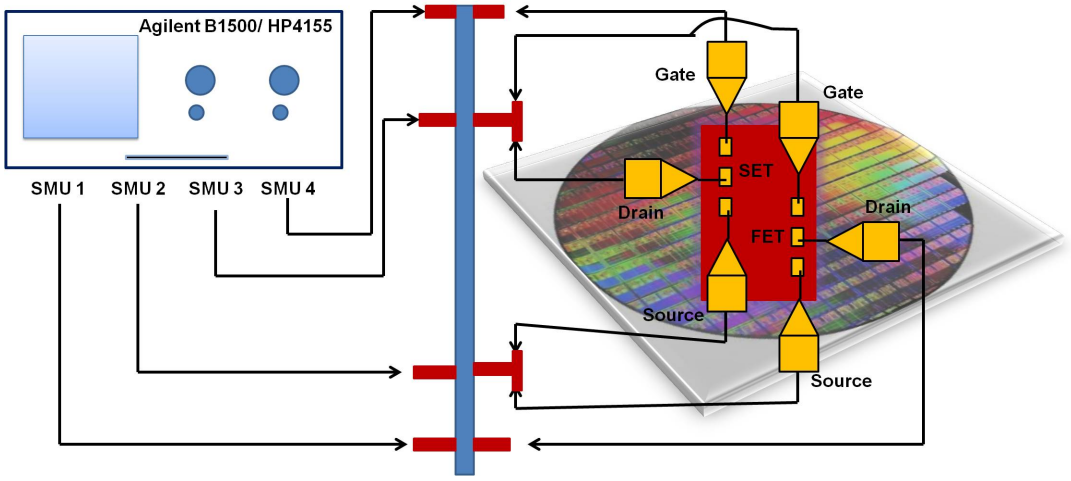


Figure A.3: Simplified schematic showing typical connections used to measure SET-FET circuits. Both the SET and the FET are on the same die of a 300 mm SOI wafer.

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